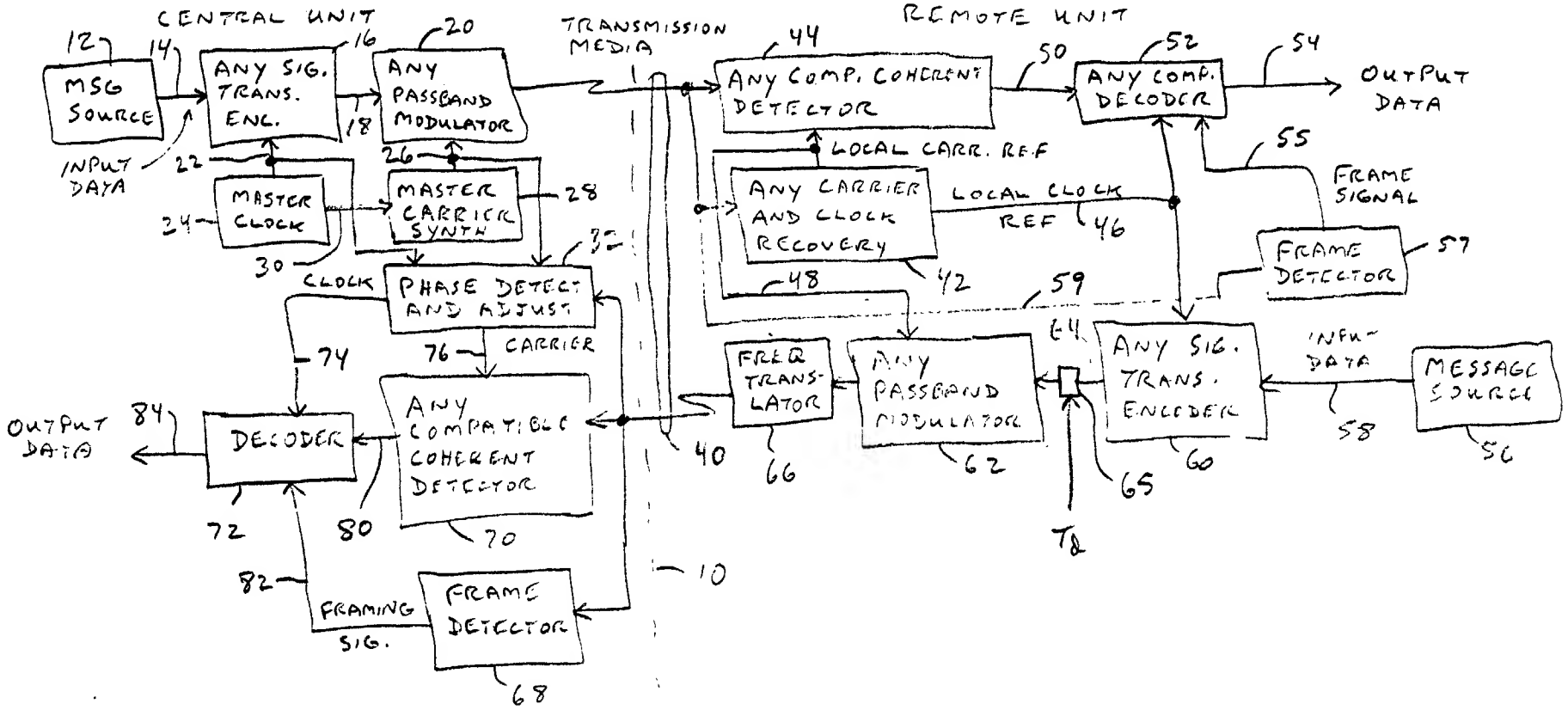
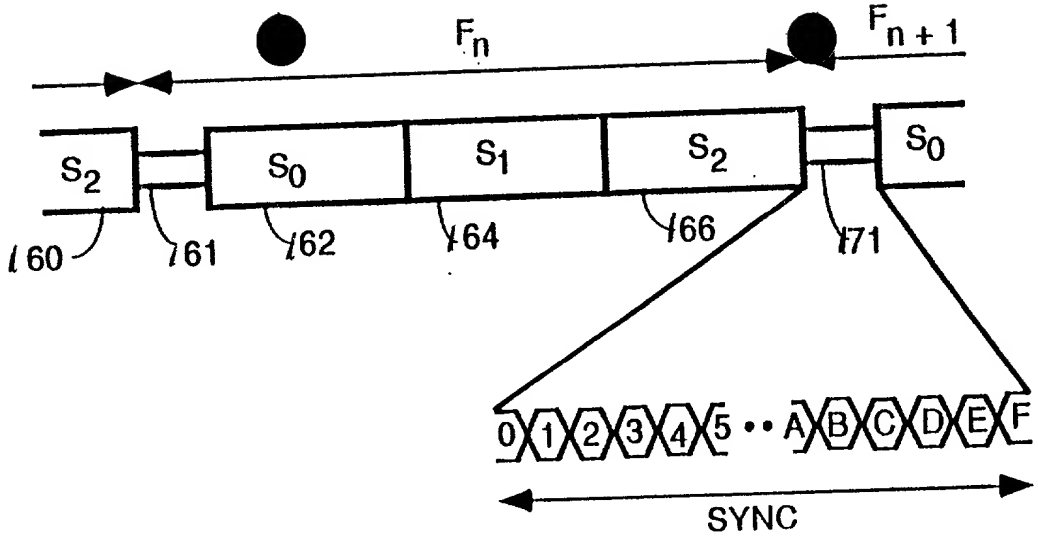
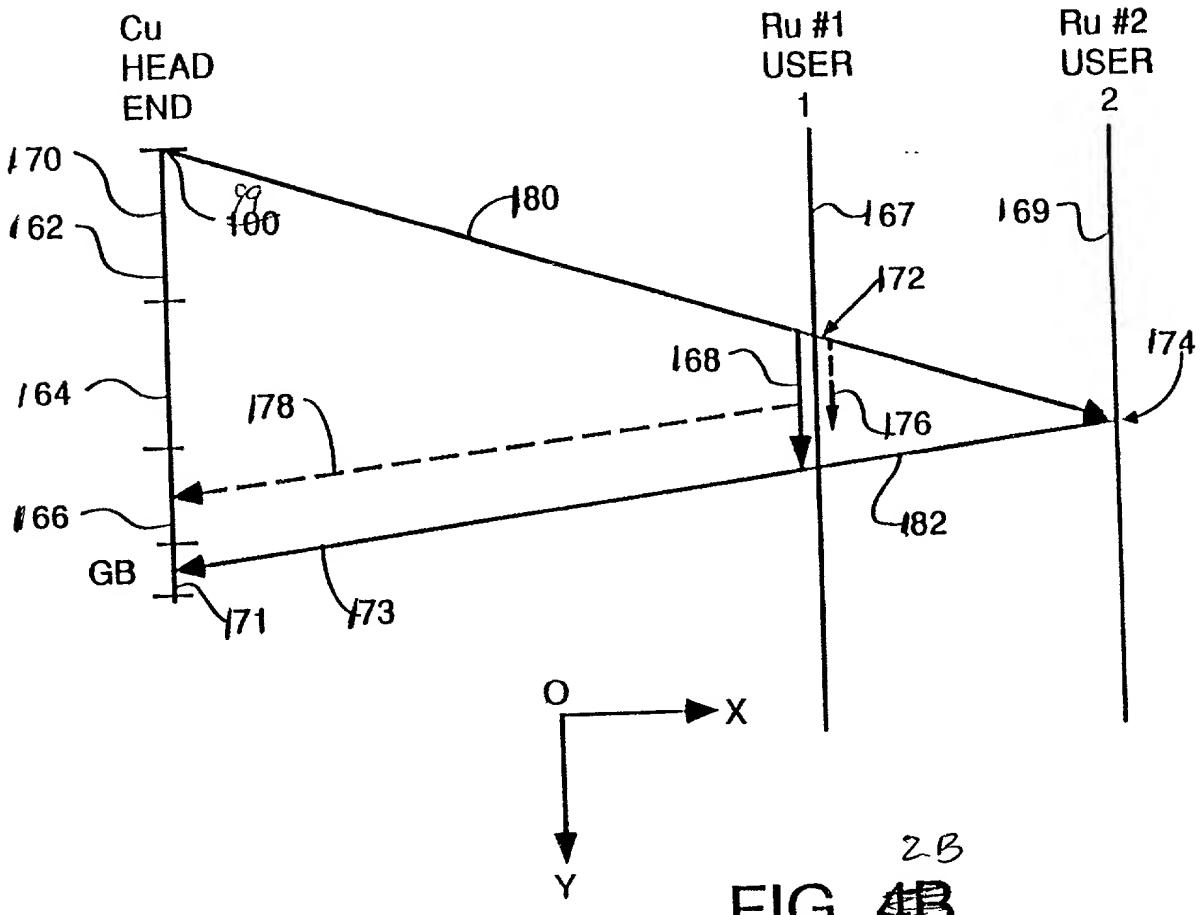


FIG. 1



2A

FIG. 4A



2B

FIG. 4B

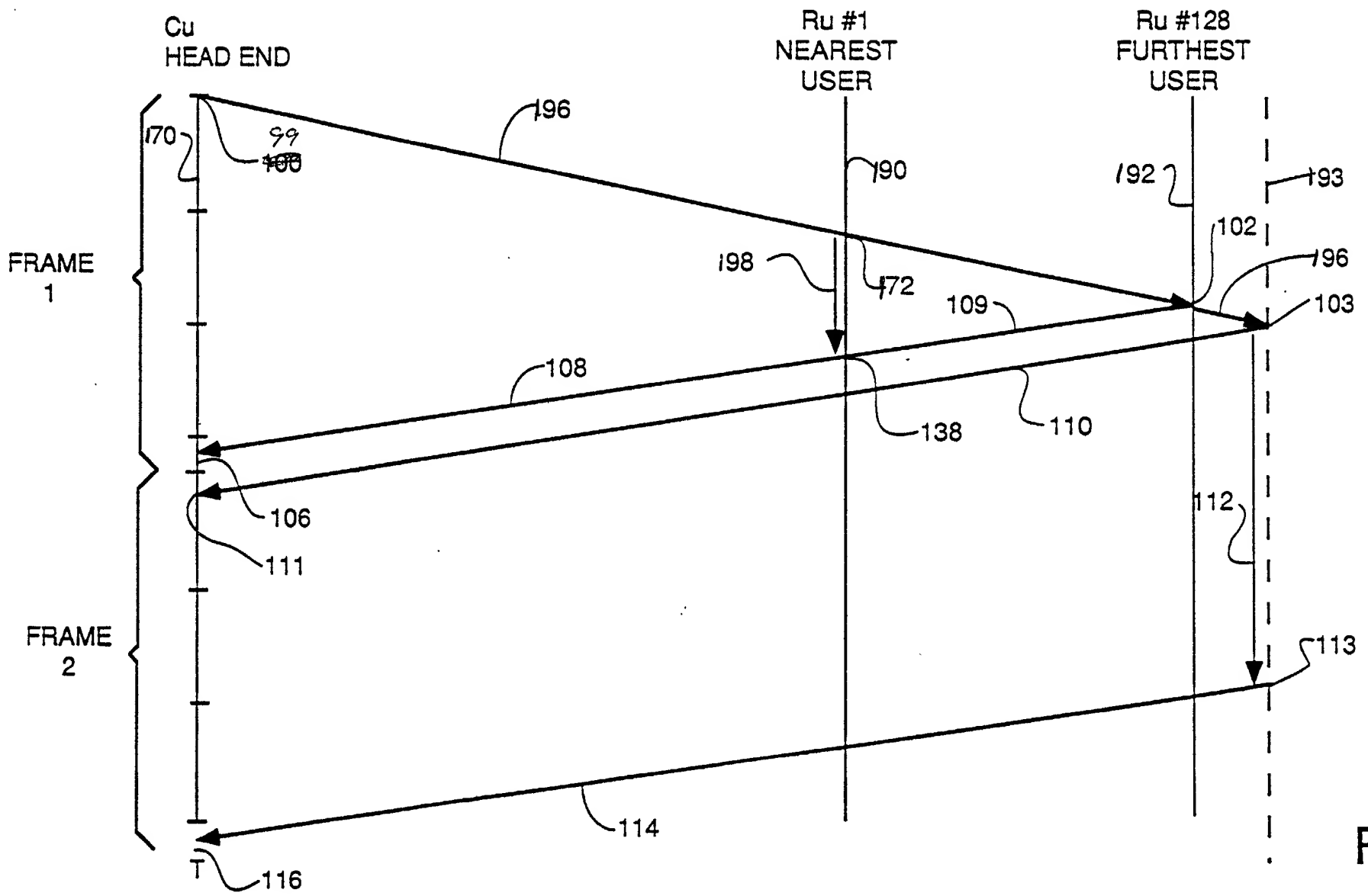


FIG. 5

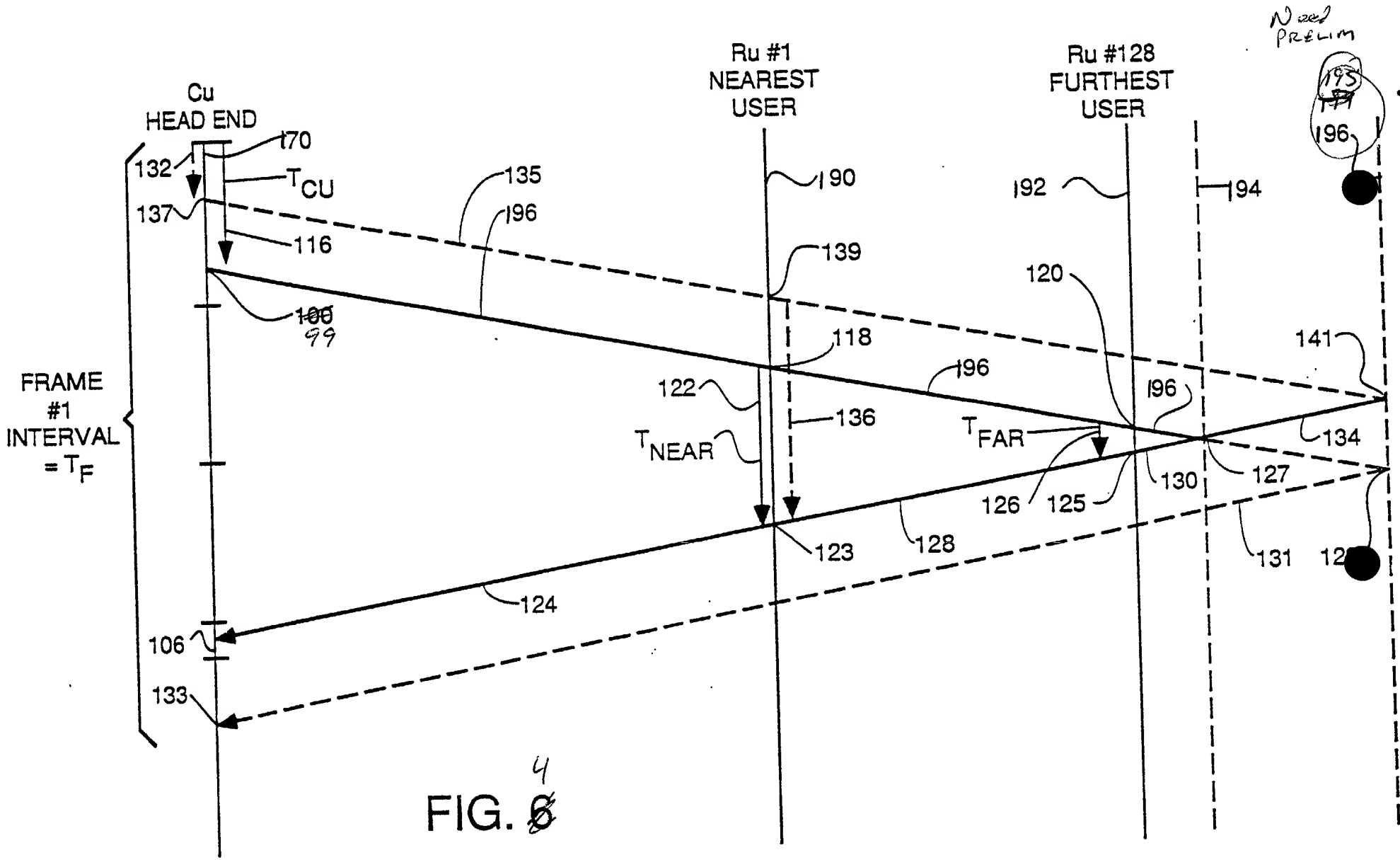
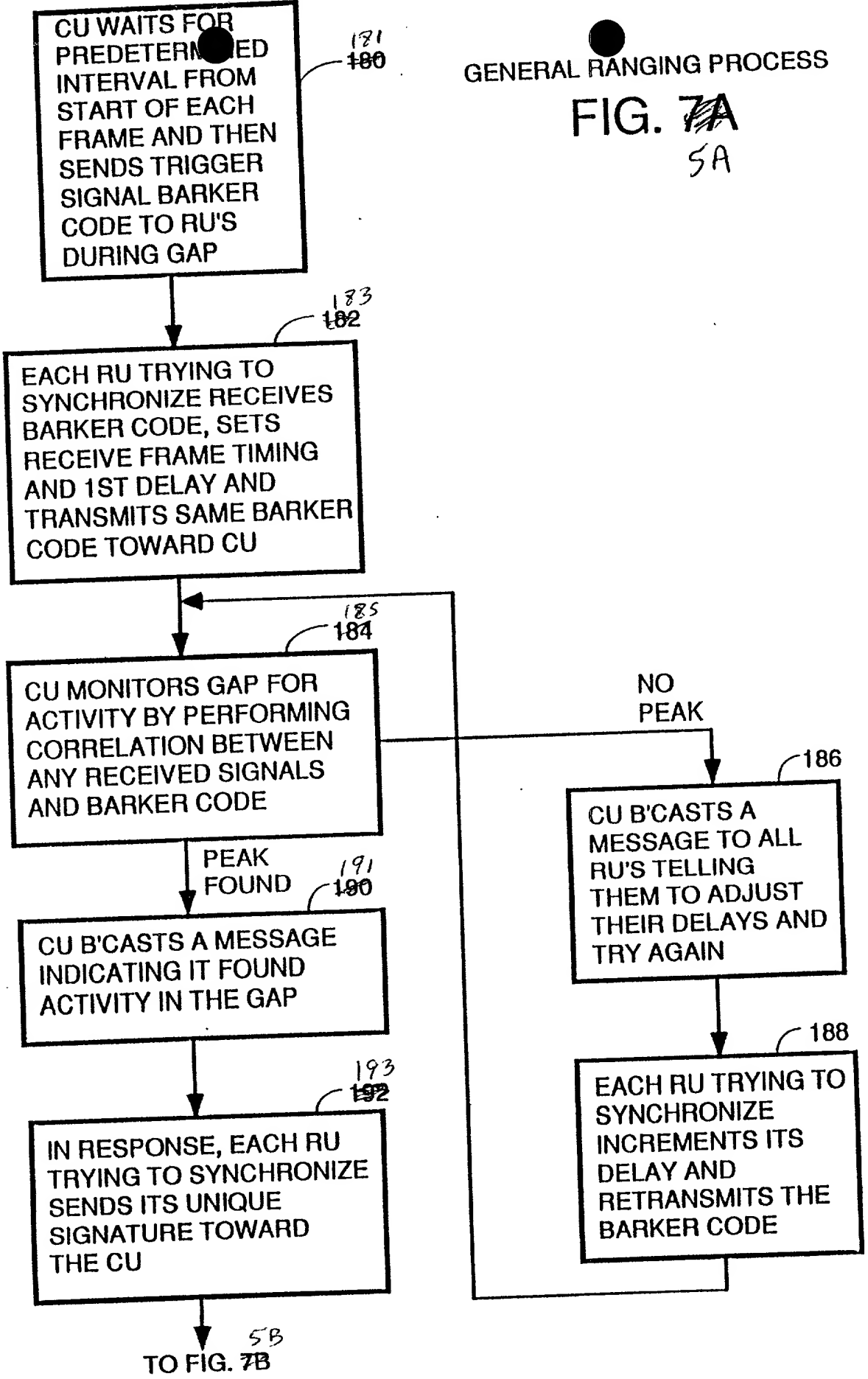

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
#1
INTERVAL
= T_F
T_{CU}
T_{NEAR}
T_{FAR}
170
132
137
116
135
196
190
192
194
139
120
118
122
136
141
134
130
127
126
125
123
128
131
124
106
133
99
Need PRELIM
195
196

FIG. 4

GENERAL RANGING PROCESS

FIG. ~~7A~~ 5A



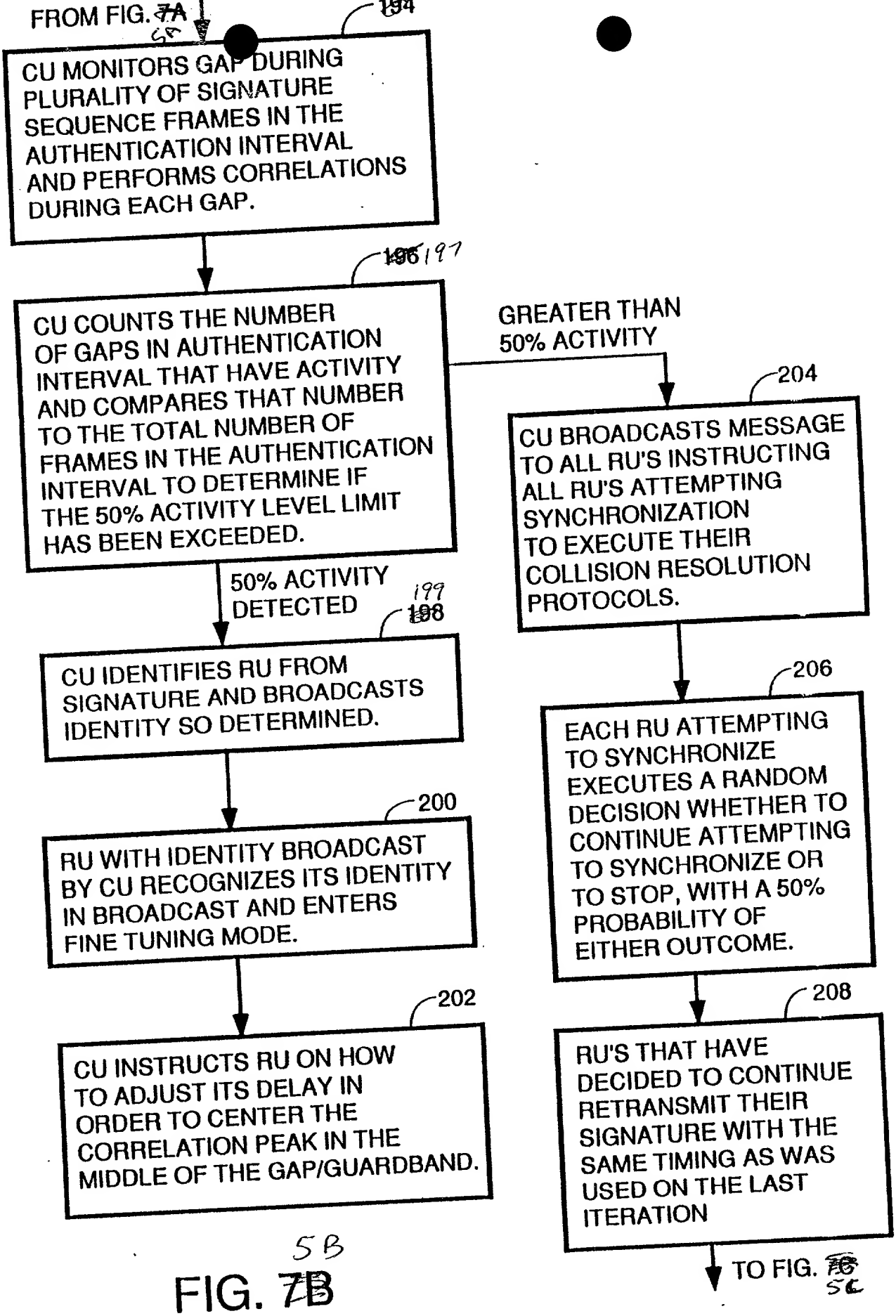

FROM FIG. 7A
CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
50% ACTIVITY DETECTED
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 5C
194
196/197
198/199
200
202
204
206
208

FIG. 7B (5B)

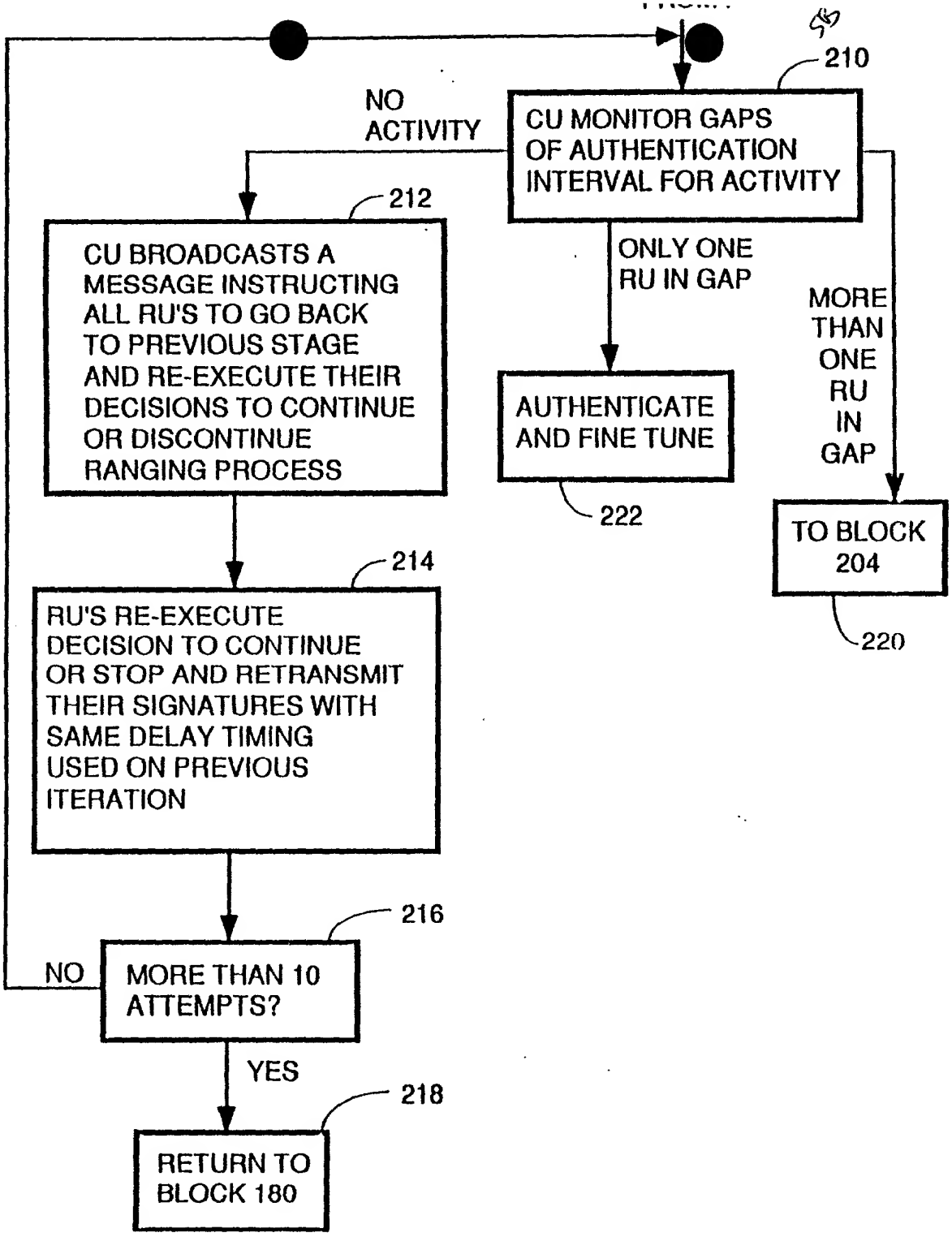
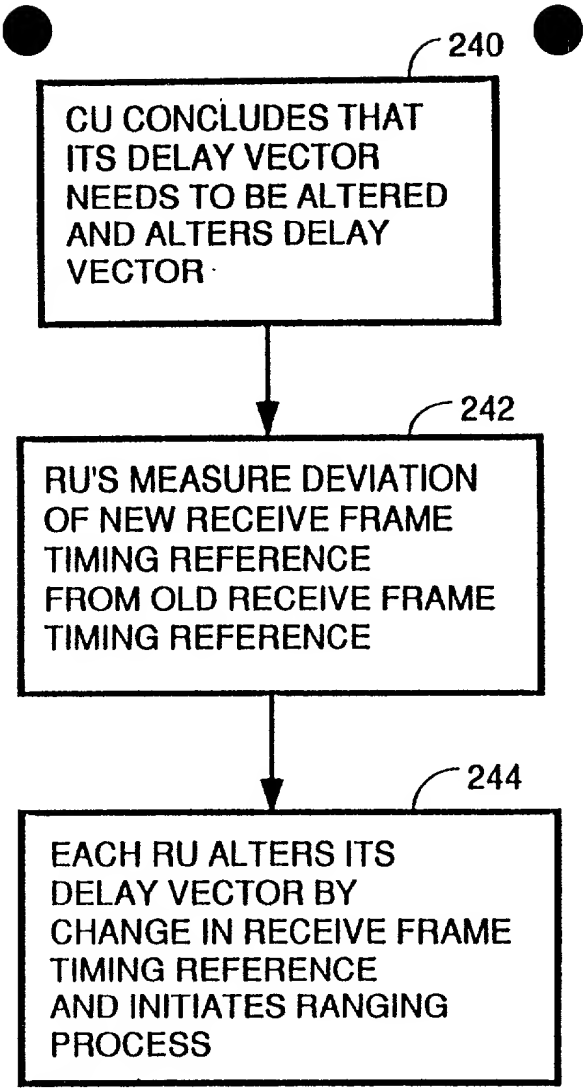

210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
ONLY ONE RU IN GAP
MORE THAN ONE RU IN GAP
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
AUTHENTICATE AND FINE TUNE
222
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 7C



6

FIG. 8

DEAD RECKONING RE-SYNC

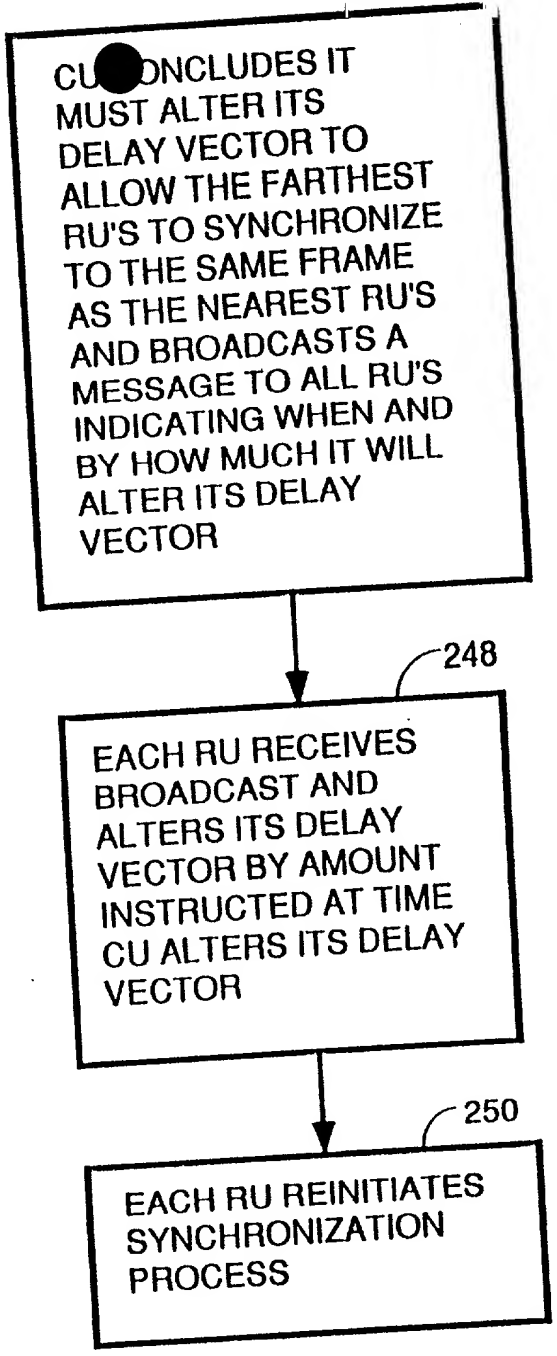
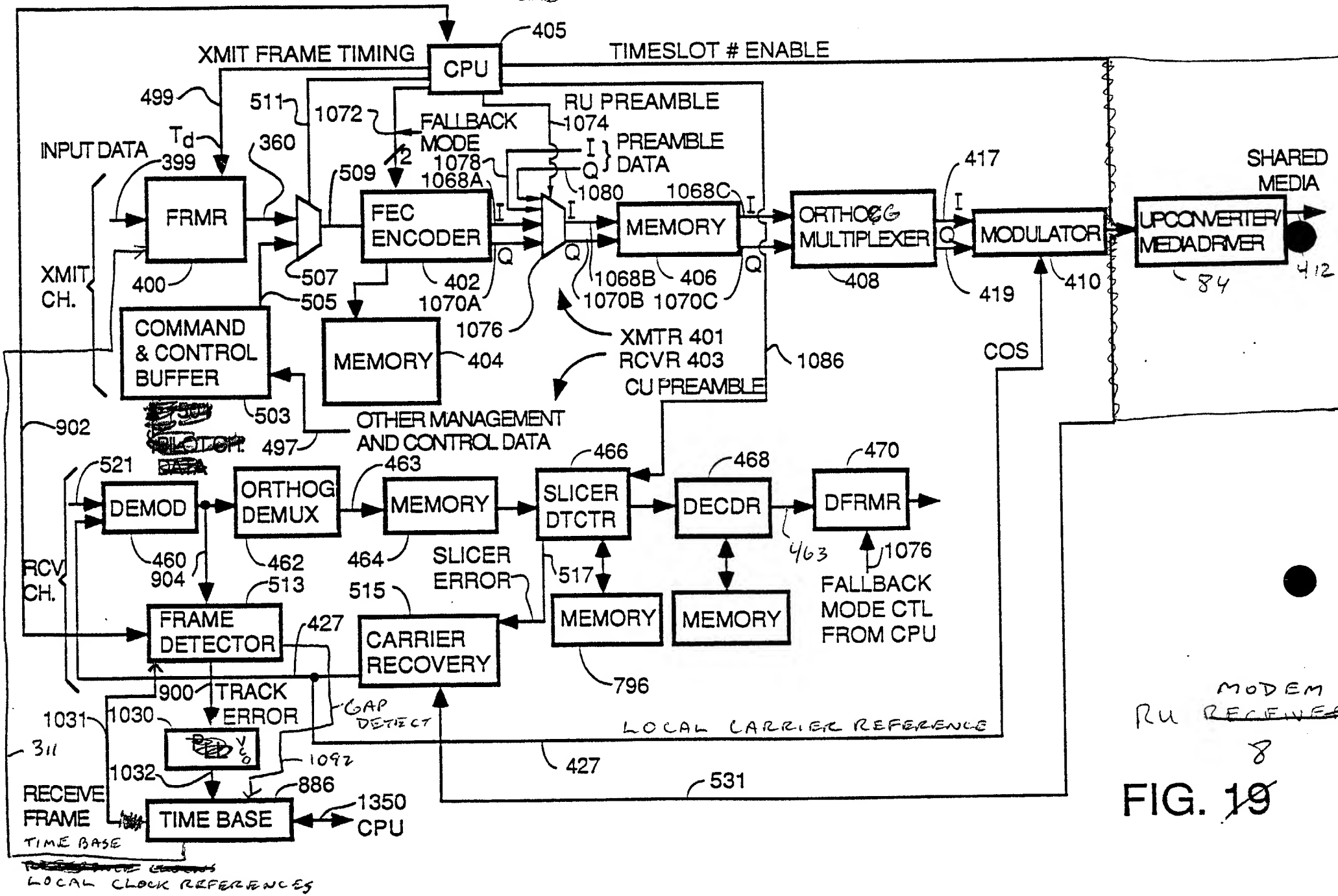


FIG. 9

PRECURSOR EMBODIMENT

DIGITAL MODEM BLOCK DIAGRAM



MODEM RU RECEIVE

8

FIG. 19

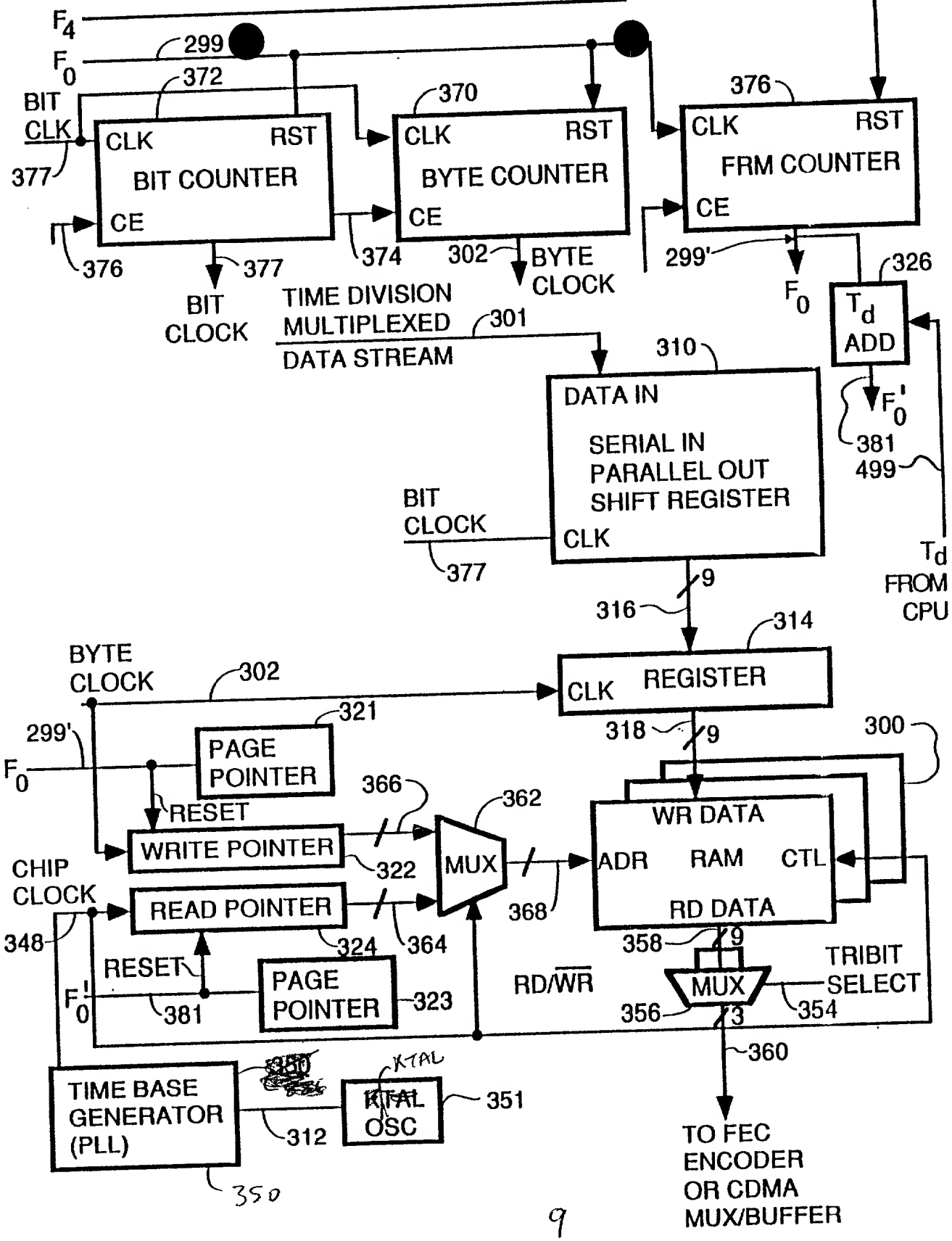

F4
F0
299
372
BIT CLK
377
CLK
RST
BIT COUNTER
CE
376
377
BIT CLOCK
374
370
CLK
RST
BYTE COUNTER
CE
302
BYTE CLOCK
376
CLK
RST
FRM COUNTER
CE
299'
F0
326
Td ADD
F'0
381
499
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
CLK
BIT CLOCK
377
Td FROM CPU
9
316
314
CLK
REGISTER
BYTE CLOCK
302
321
299'
F0
PAGE POINTER
RESET
366
362
WRITE POINTER
322
MUX
CHIP CLOCK
READ POINTER
324
364
348
RESET
F!0
381
PAGE POINTER
323
368
318
9
300
WR DATA
ADR
RAM
CTL
RD DATA
358
9
RD/WR
MUX
356
3
TRIBIT SELECT
354
360
TIME BASE GENERATOR (PLL)
312
XTAL
OSC
351
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 12

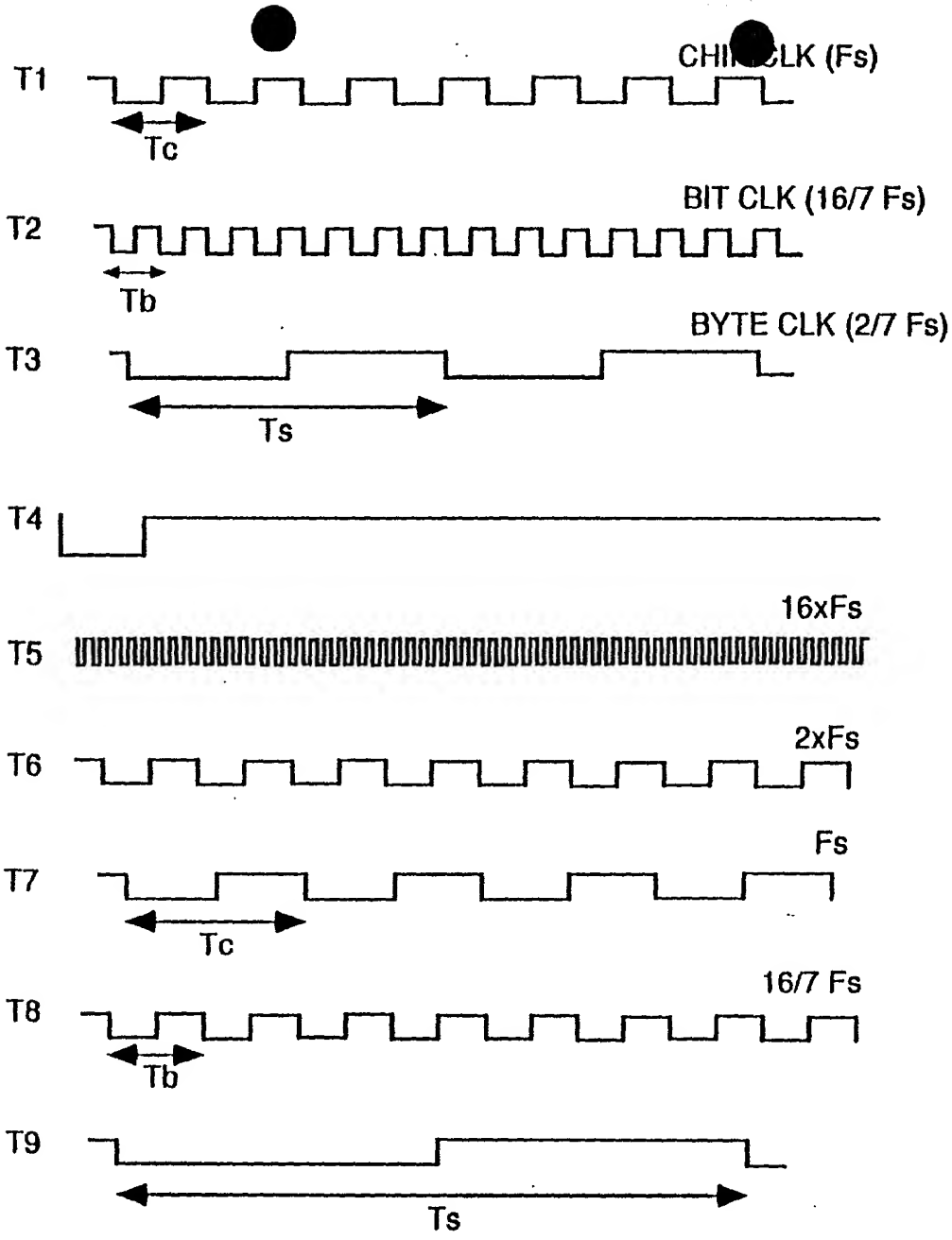
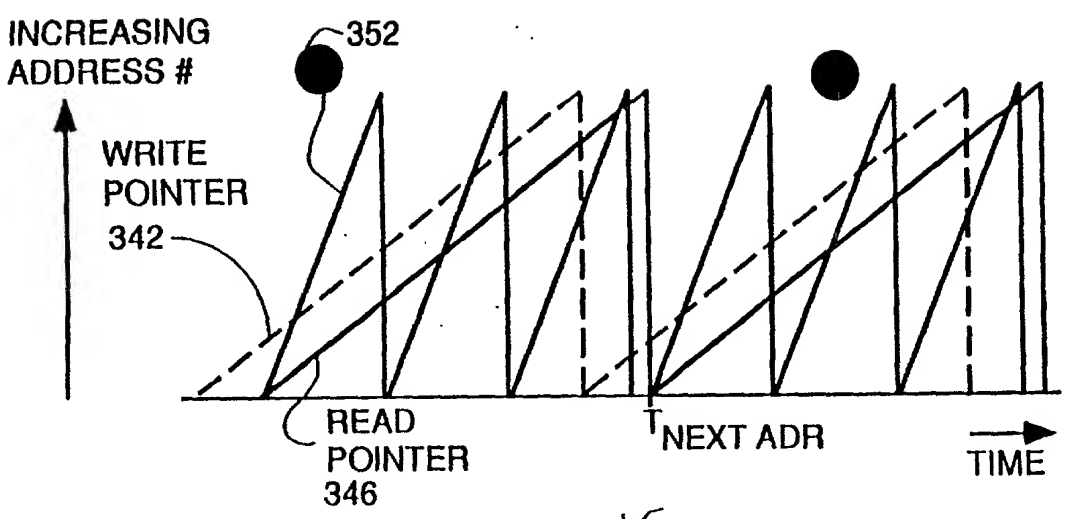
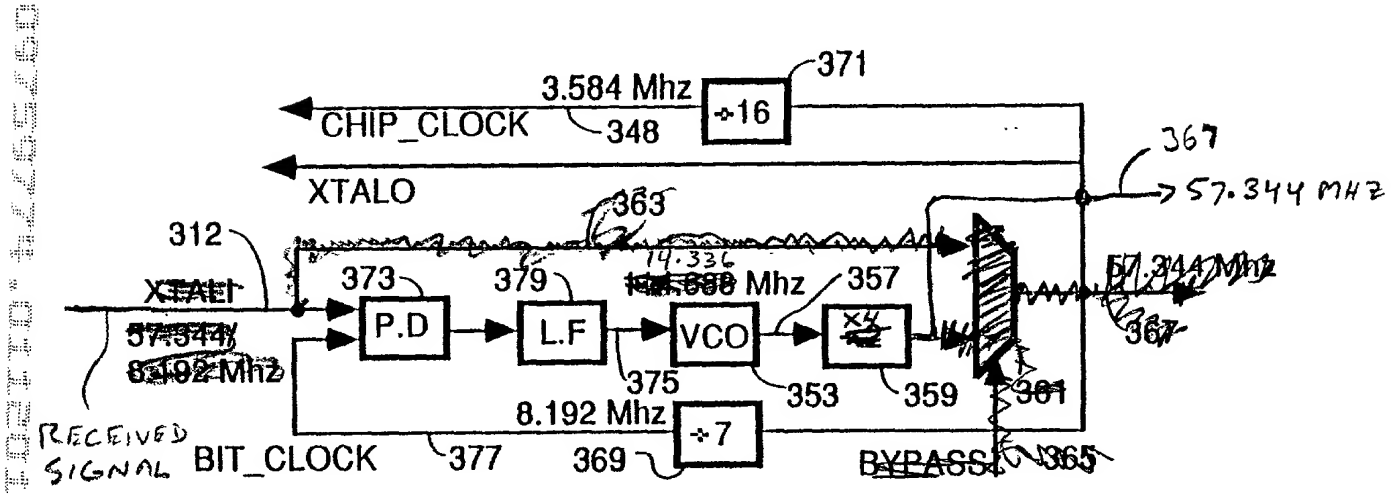

T1
CHI CLK (Fs)
Tc
T2
BIT CLK (16/7 Fs)
Tb
T3
BYTE CLK (2/7 Fs)
Ts
T4
T5
16xFs
T6
2xFs
T7
Fs
Tc
T8
16/7 Fs
Tb
T9
Ts

FIG. 13



15

FIG. ~~17~~



11

FIG. ~~18~~

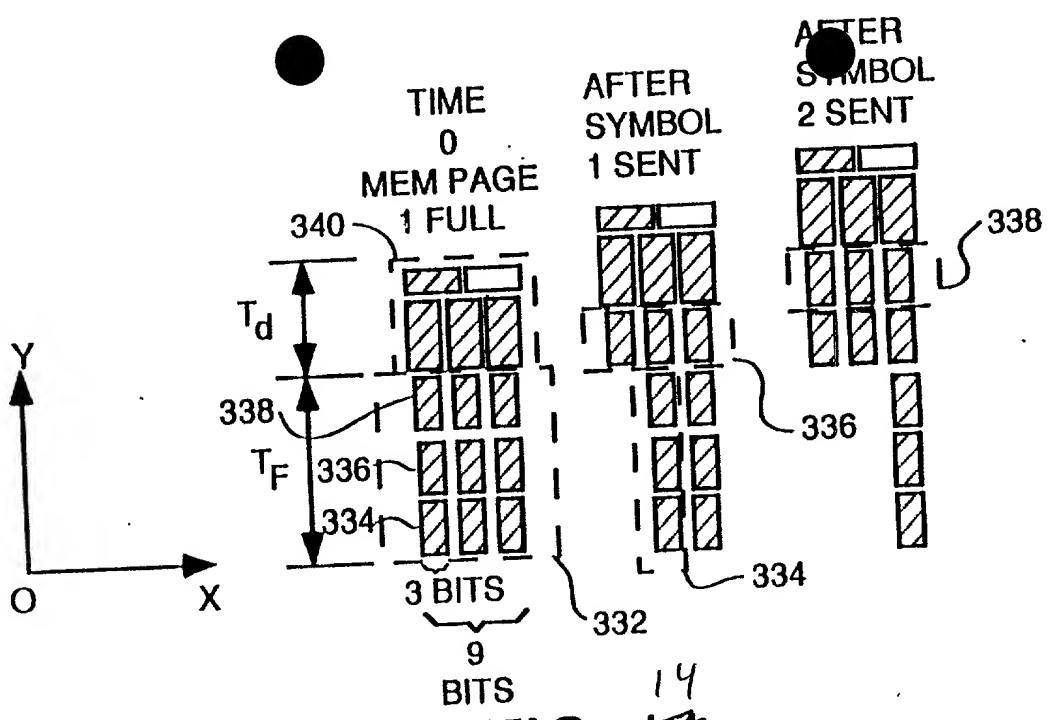


FIG. 14

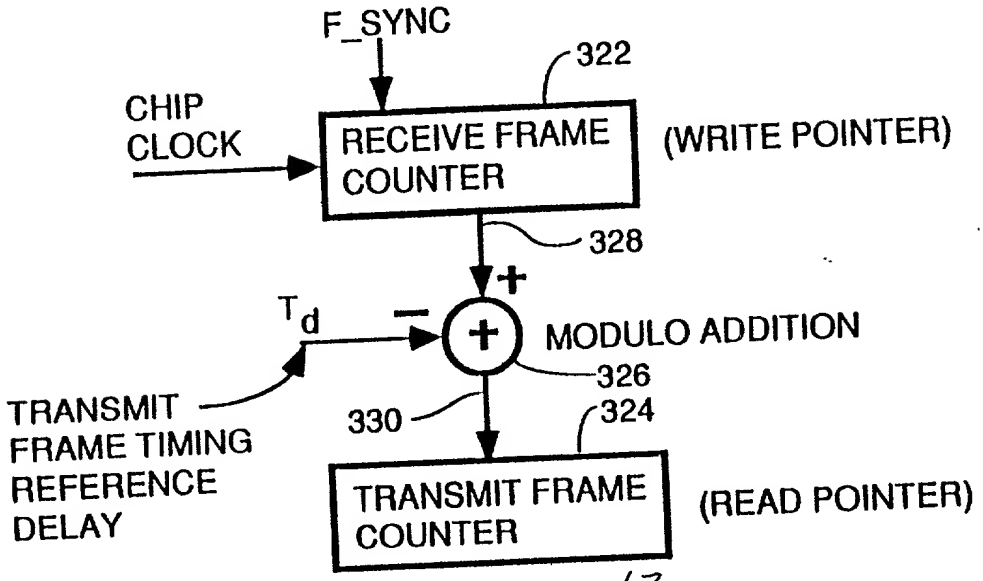


FIG. 15

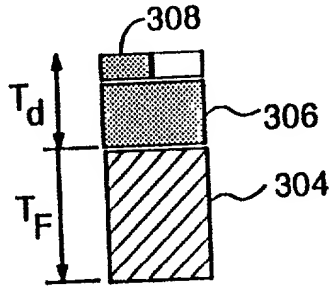


FIG. 16

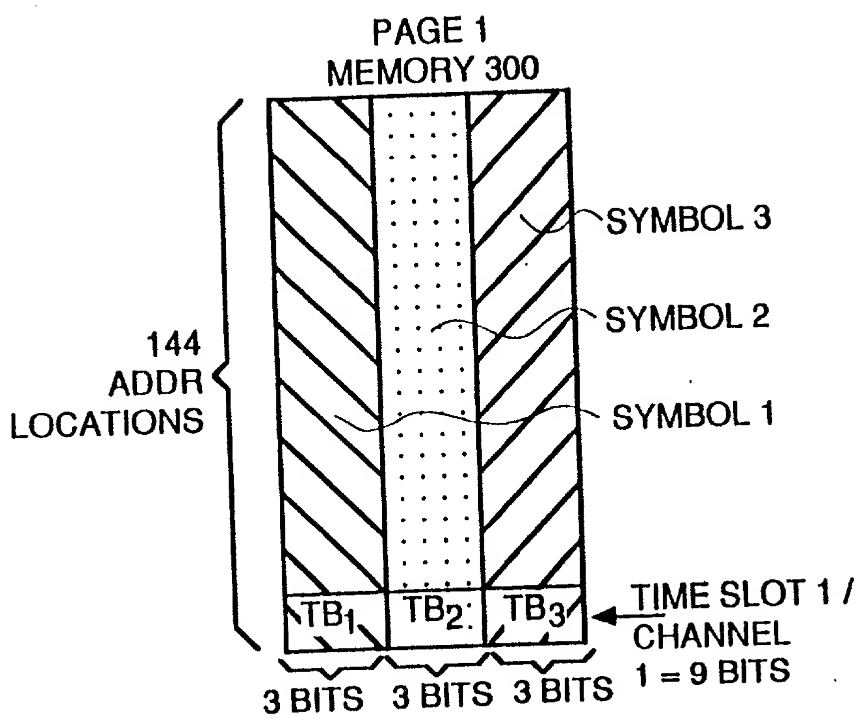
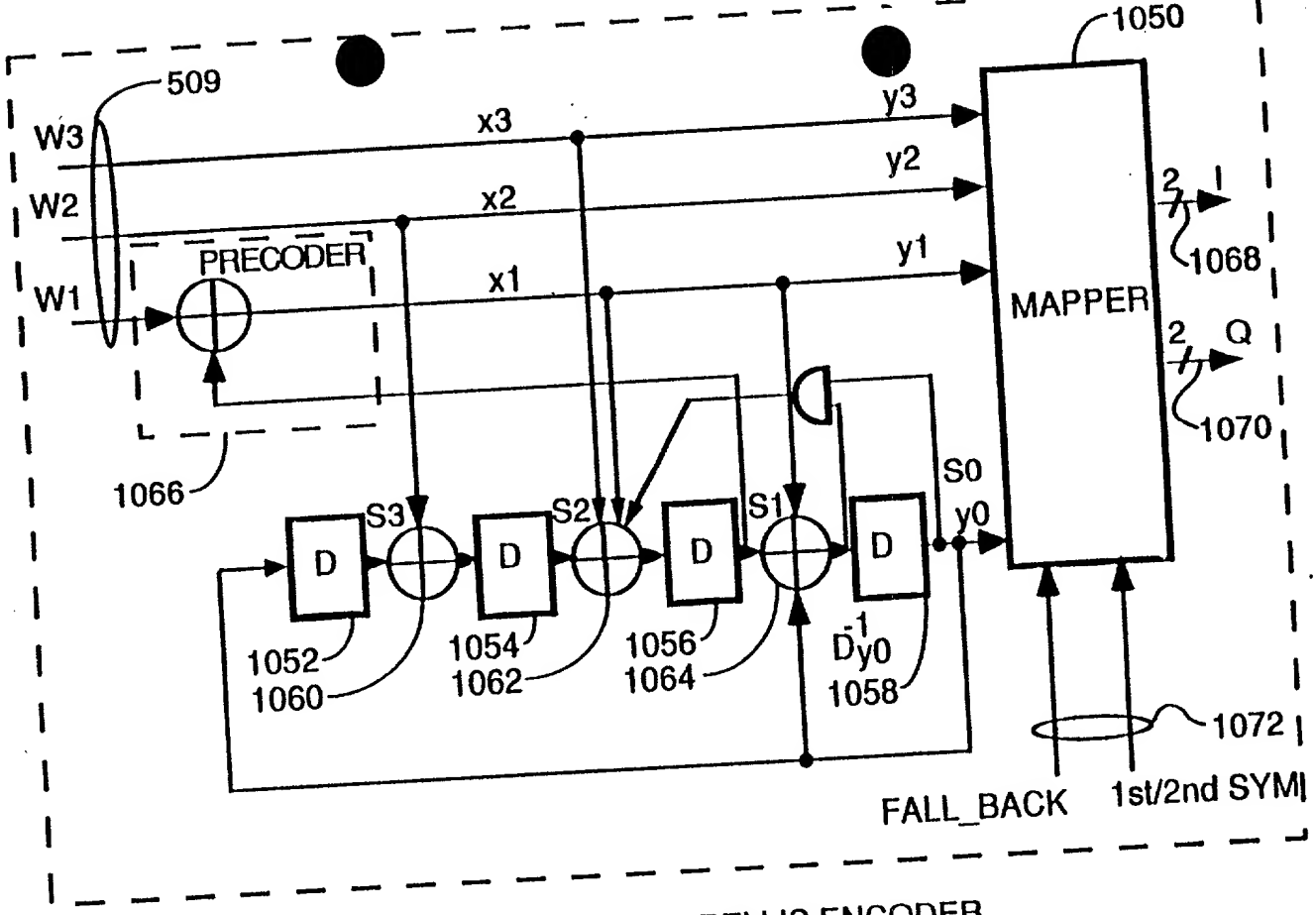

PAGE 1
MEMORY 300
SYMBOL 3
SYMBOL 2
SYMBOL 1
144
ADDR
LOCATIONS
TB_1
TB_2
TB_3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. ~~20~~ 16

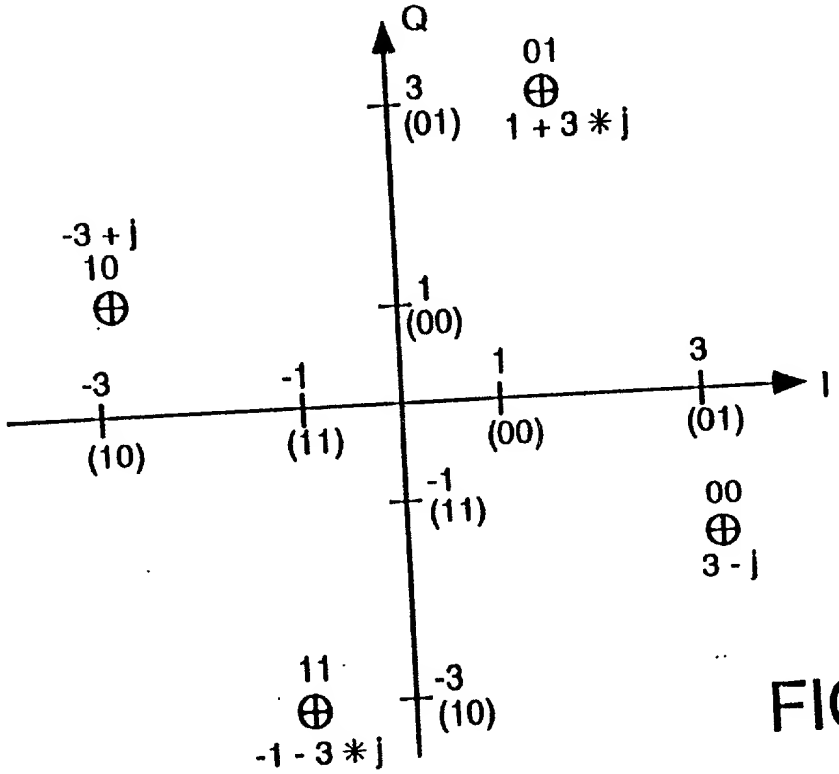


PREFERRED TRELLIS ENCODER

FIG. 42

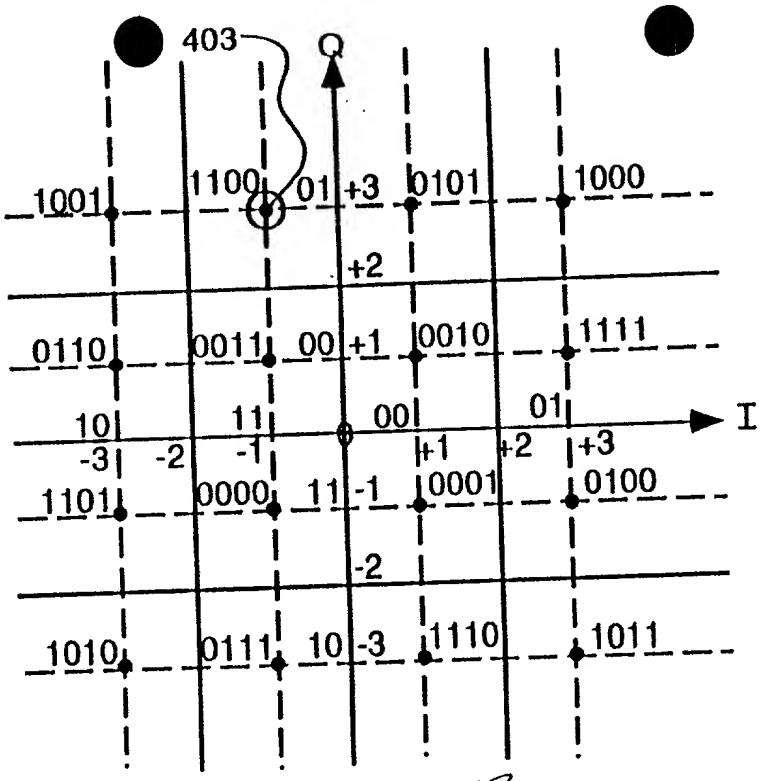
17

MAPPING FOR FALL-BACK MODE - LSB'S



21

FIG. 43



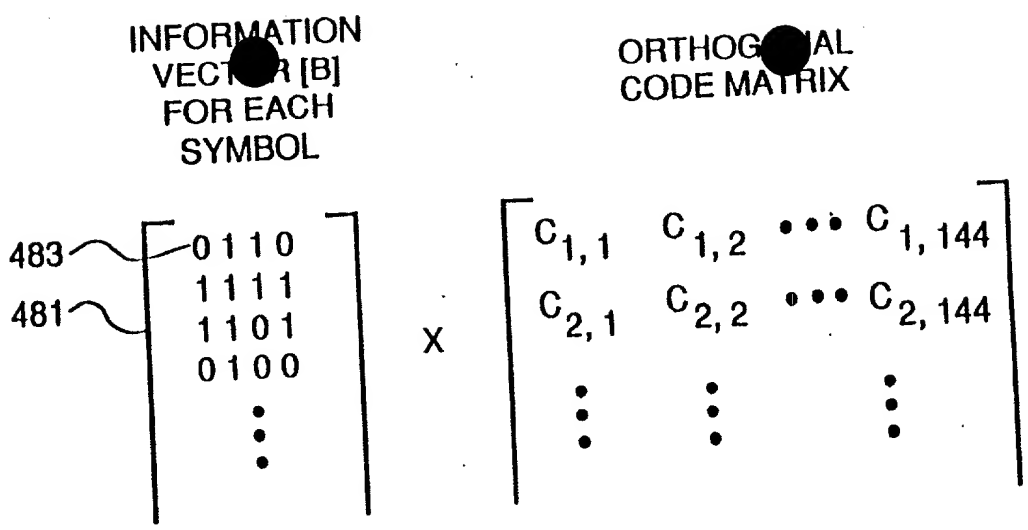
18

FIG. 21

CODE	INPHASE	QUADRATURE	
0000	111	111	= -1 - j
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3* j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3* j
1000	011	011	=+3 + 3* j
1001	101	011	= -3 + 3* j
1010	101	101	= -3 - 3* j
1011	011	101	= 3 - 3* j
1100 (403)	111	011	= -1+ 3* j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3* j
1111	011	001	= 3 + j

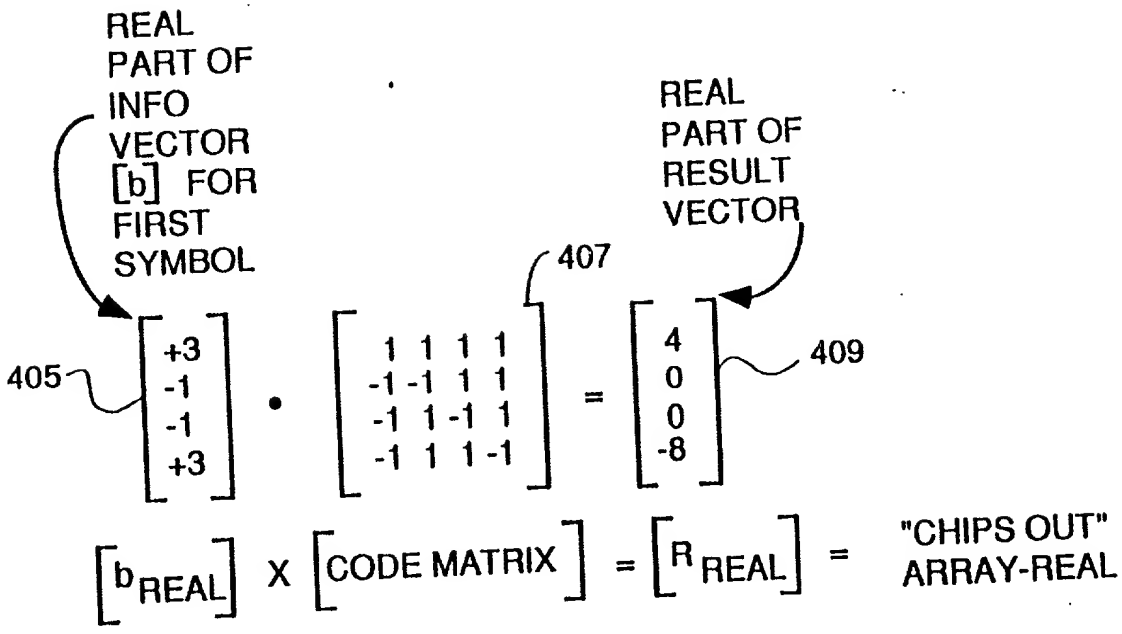
19

FIG. 22



20A

FIG. ~~23~~A



20B

FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~44~~ 22

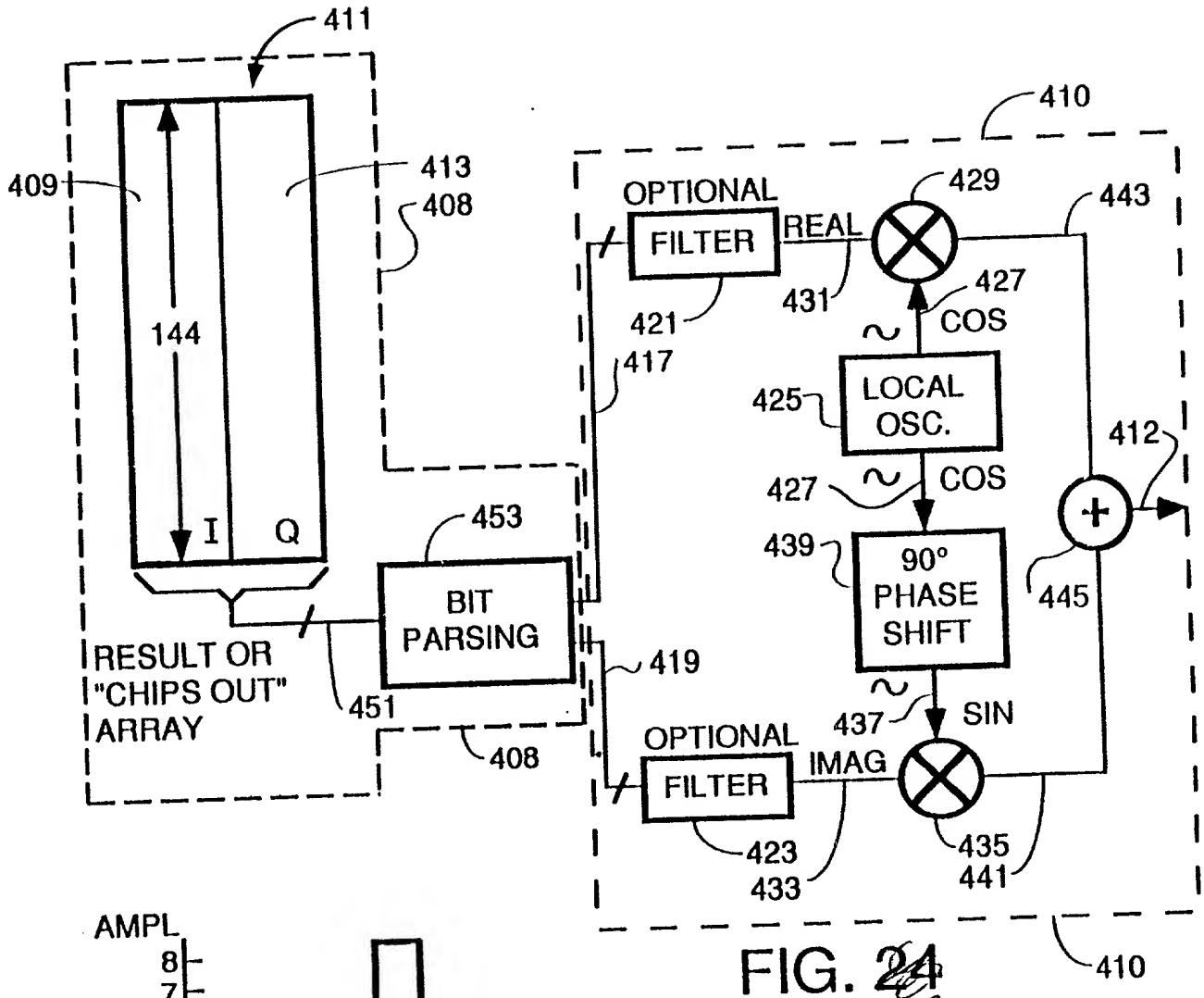
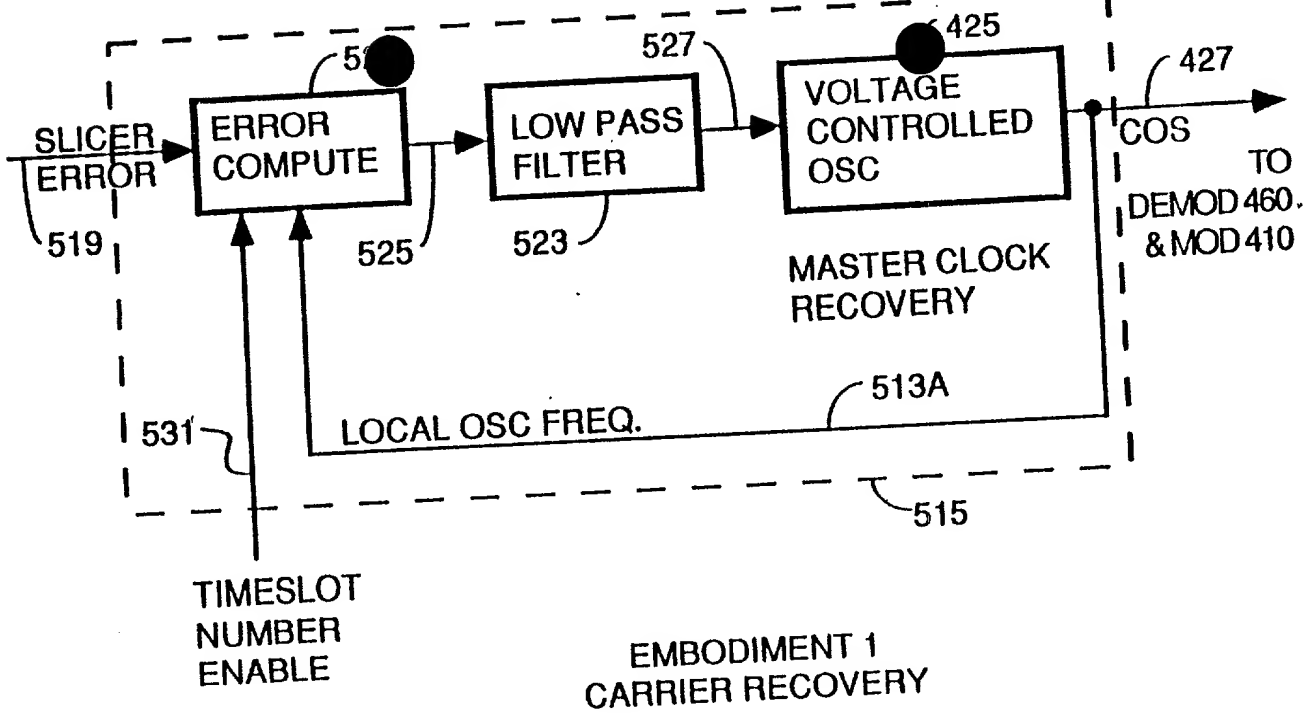

411
409
413
408
144
I
Q
453
BIT
PARSING
RESULT OR
"CHIPS OUT"
ARRAY
451
408
410
OPTIONAL
FILTER
REAL
421
429
431
443
427
COS
417
425
LOCAL
OSC.
412
427
COS
439
90°
PHASE
SHIFT
445
419
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 24


AMPL
8
7
6
5
4
3
2
1
0
TIME

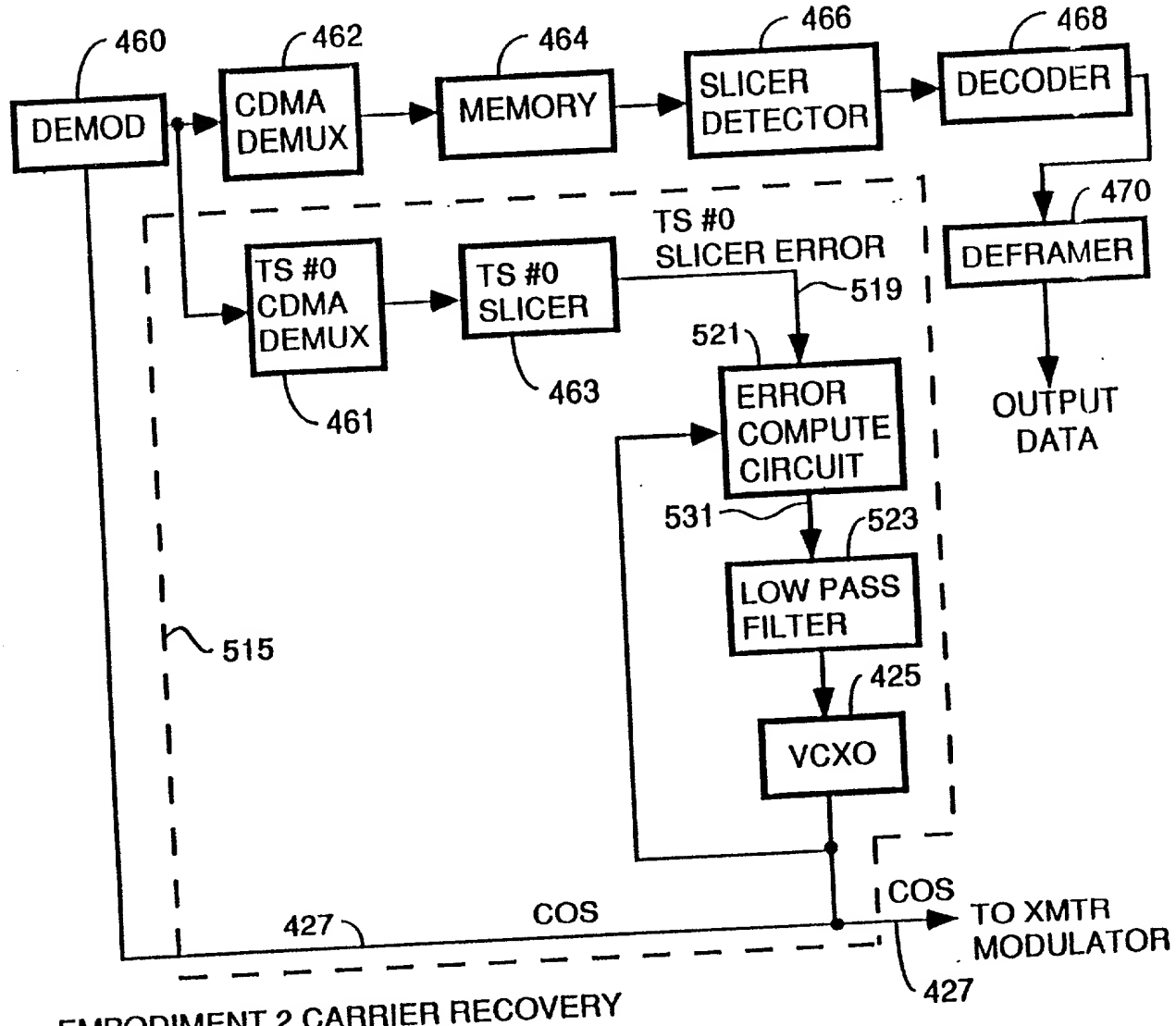
FIG. 25



EMBODIMENT 1
CARRIER RECOVERY

FIG. 35

25



EMBODIMENT 2 CARRIER RECOVERY

FIG. 36

26

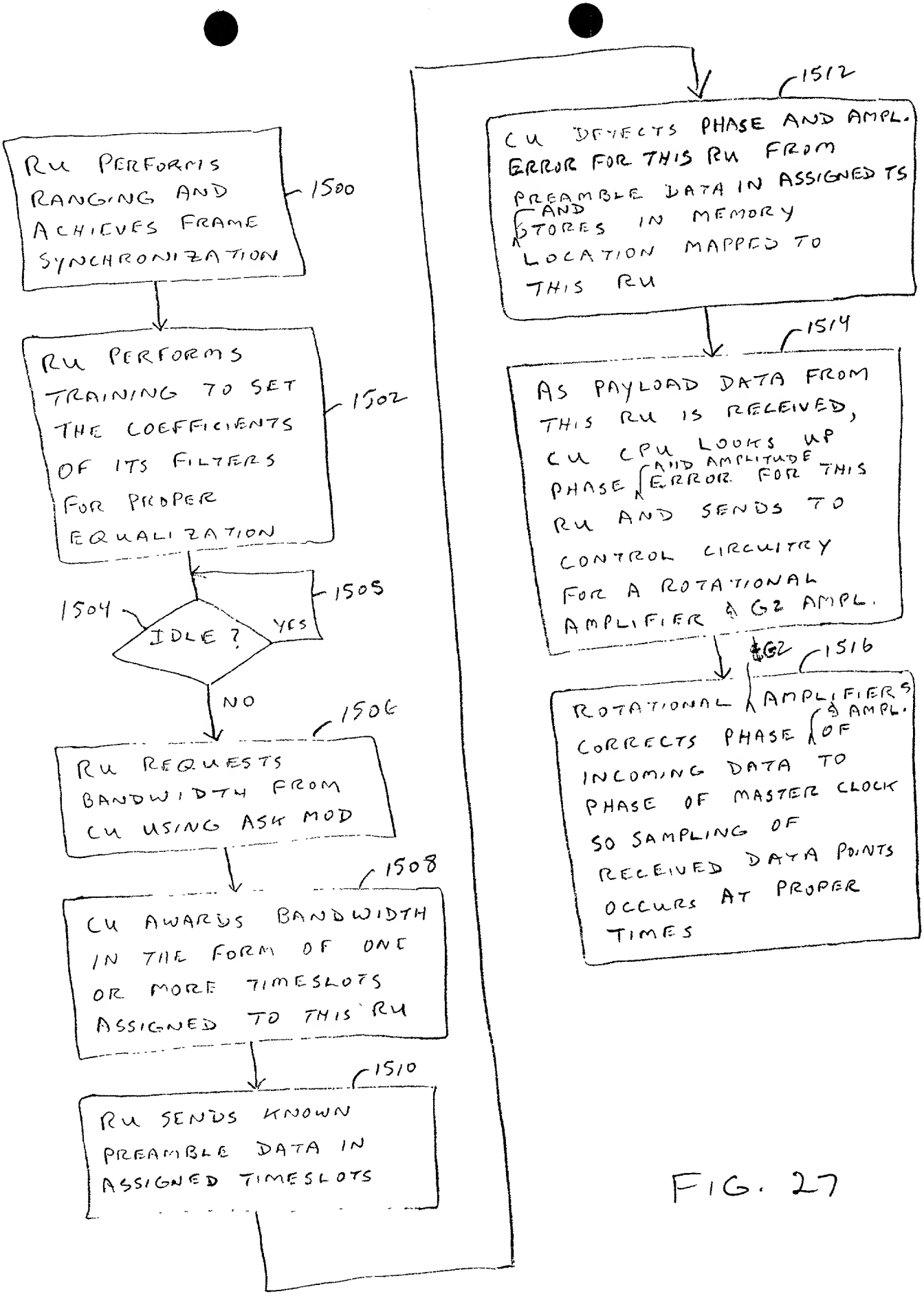
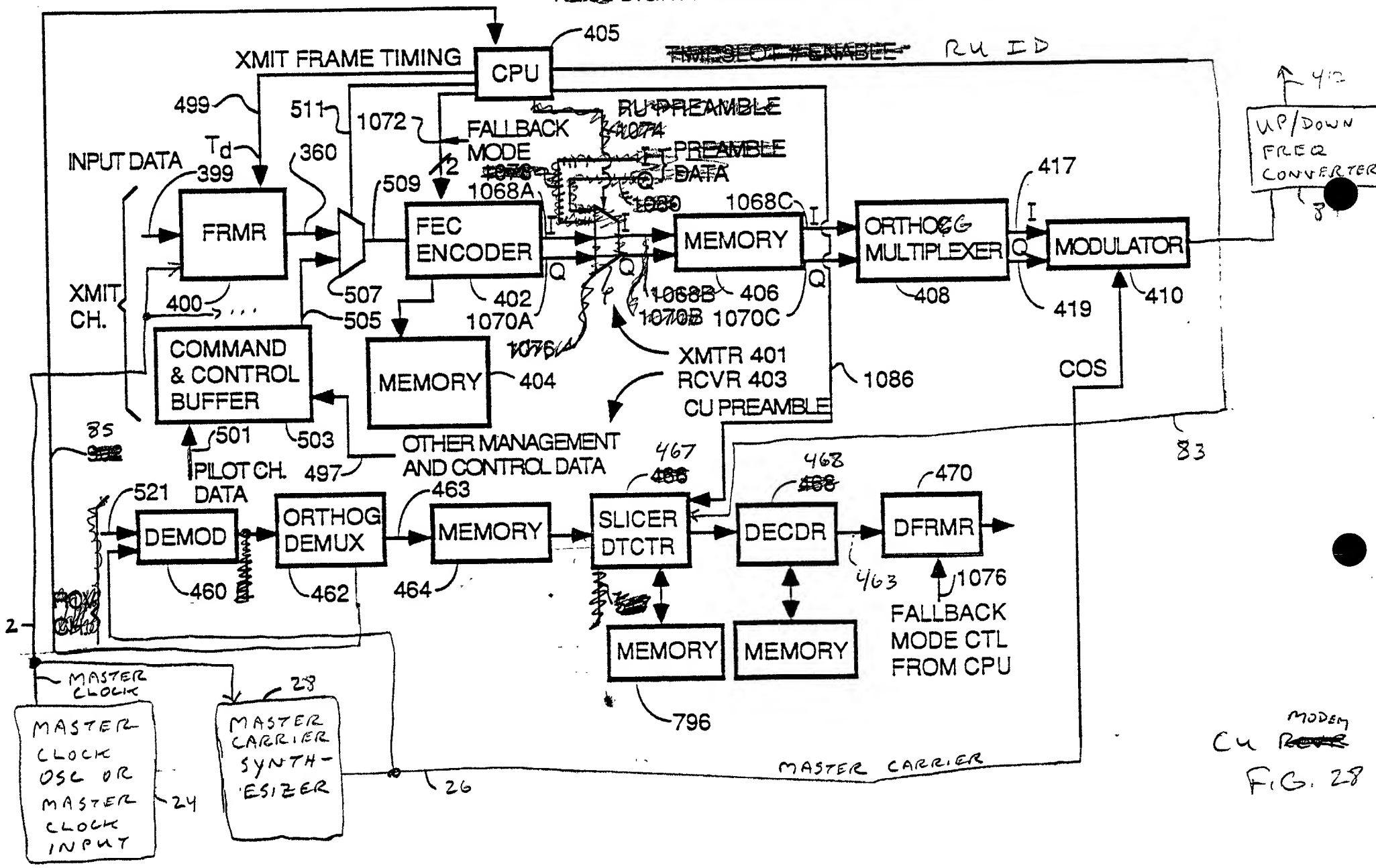

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1506
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1508
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1510
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1512
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1514
ROTATIONAL AMPLIFIERS & G2 AMPL. CORRECTS PHASE OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES
1516

FIG. 27

CU

DIGITAL MODEM BLOCK DIAGRAM



CU MODEM

FIG. 28

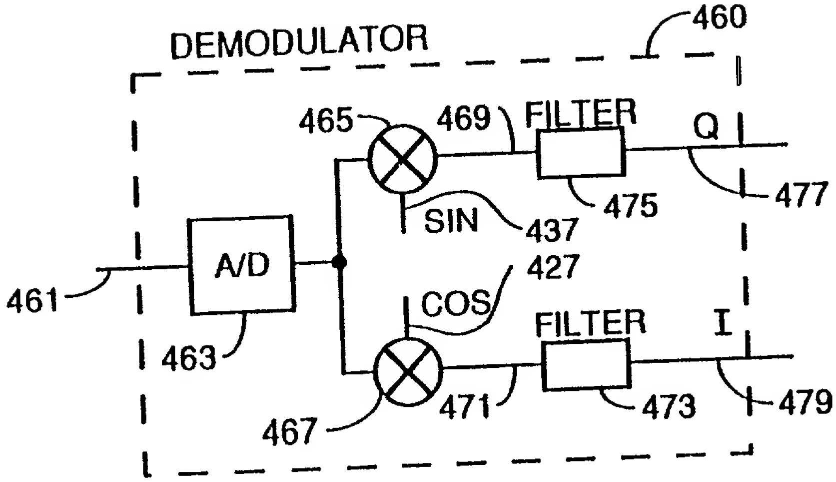


FIG. ~~26~~ 29

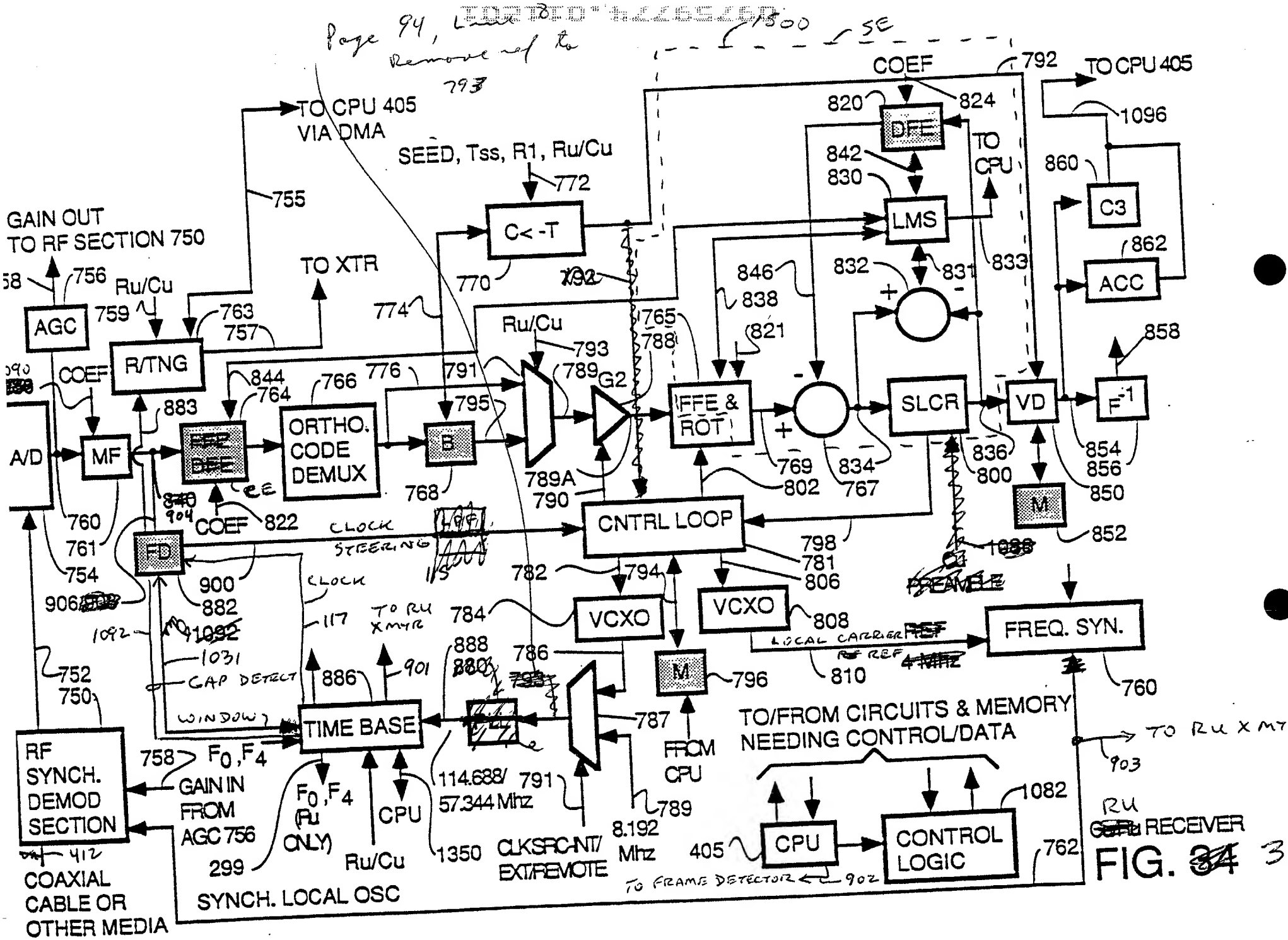

TO CPU 405 VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
C<--T
1500
5E
COEF
792
TO CPU 405
820
824
DFE
1096
842
830
TO CPU
LMS
860
C3
GAIN OUT TO RF SECTION 750
TO XTR
770
774
Ru/Cu
793
765
788
846
838
832
831
833
862
ACC
AGC
759
763
757
R/TNG
Ru/Cu
858
COEF
844
764
766
776
791
789
G2
795
821
FFE & ROT
SLCR
VD
F-1
A/D
MF
883
FFE
DFE
ORTHO. CODE DEMUX
B
768
789A
790
769
834
767
802
836
800
854
856
850
M
852
760
761
754
906
904
COEF
822
CLOCK STEERING
CNTRL LOOP
798
781
806
FD
900
882
CLOCK
782
794
784
VCXO
VCXO
808
FREQ. SYN.
1092
1031
117
TO RU XMTR
888
786
752
750
CAP DETECT
886
901
M
796
LOCAL CARRIER REF
RF REF 4 Mhz
810
760
WINDOW
TIME BASE
787
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
FROM CPU
TO RU XMTR
903
758
F0, F4
GAIN IN FROM AGC 756
F0, F4 (Rx ONLY)
CPU
114.688/ 57.344 Mhz
791
789
8.192 Mhz
1350
CLKSRC-INT/ EXT/REMOTE
405
CPU
CONTROL LOGIC
1082
762
RU RECEIVER
RF SYNCH. DEMOD SECTION
412
COAXIAL CABLE OR OTHER MEDIA
299
SYNCH. LOCAL OSC
Ru/Cu
TO FRAME DETECTOR
902

FIG. 30

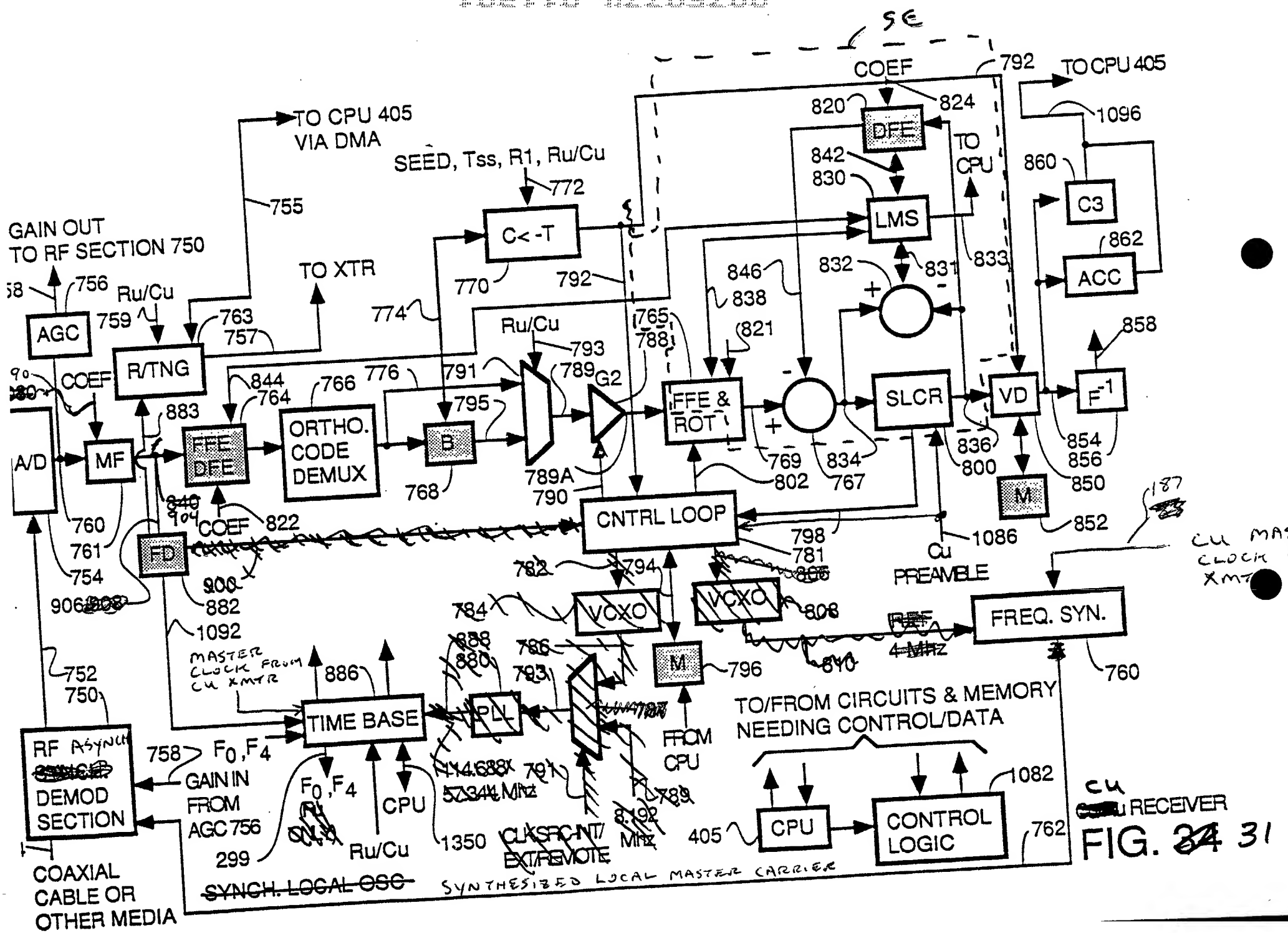

TO CPU 405
VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
GAIN OUT
TO RF SECTION 750
TO XTR
AGC
759
R/TNG
763
757
Ru/Cu
756
COEF
844
764
883
A/D
MF
FFE
DFE
ORTHO.
CODE
DEMUX
766
776
791
795
B
768
789A
790
789
G2
793
774
770
C<-T
792
765
788
821
838
846
FFE &
ROT
769
834
767
802
LMS
820
DFE
842
830
832
831
833
TO
CPU
SLCR
836
800
VD
M
852
CNTRL LOOP
798
781
794
782
784
VCXO
VCXO
808
FREQ. SYN.
4 MHz
760
752
750
RF ASYNCH
DEMOD
SECTION
758
GAIN IN
FROM
AGC 756
COAXIAL
CABLE OR
OTHER MEDIA
TIME BASE
886
299
Ru/Cu
1350
CPU
PLL
786
793
791
789
FROM
CPU
TO/FROM CIRCUITS & MEMORY
NEEDING CONTROL/DATA
CPU
405
CONTROL
LOGIC
1082
762
C3
860
ACC
862
858
F-1
854
856
850
1086
Cu
PREAMBLE
1092
882
754
761
760
906
904
900
822
COEF
FD
MASTER
CLOCK FROM
CU XMTR
SYNTHESIZED LOCAL MASTER CARRIER
Cu RECEIVER

FIG. 31

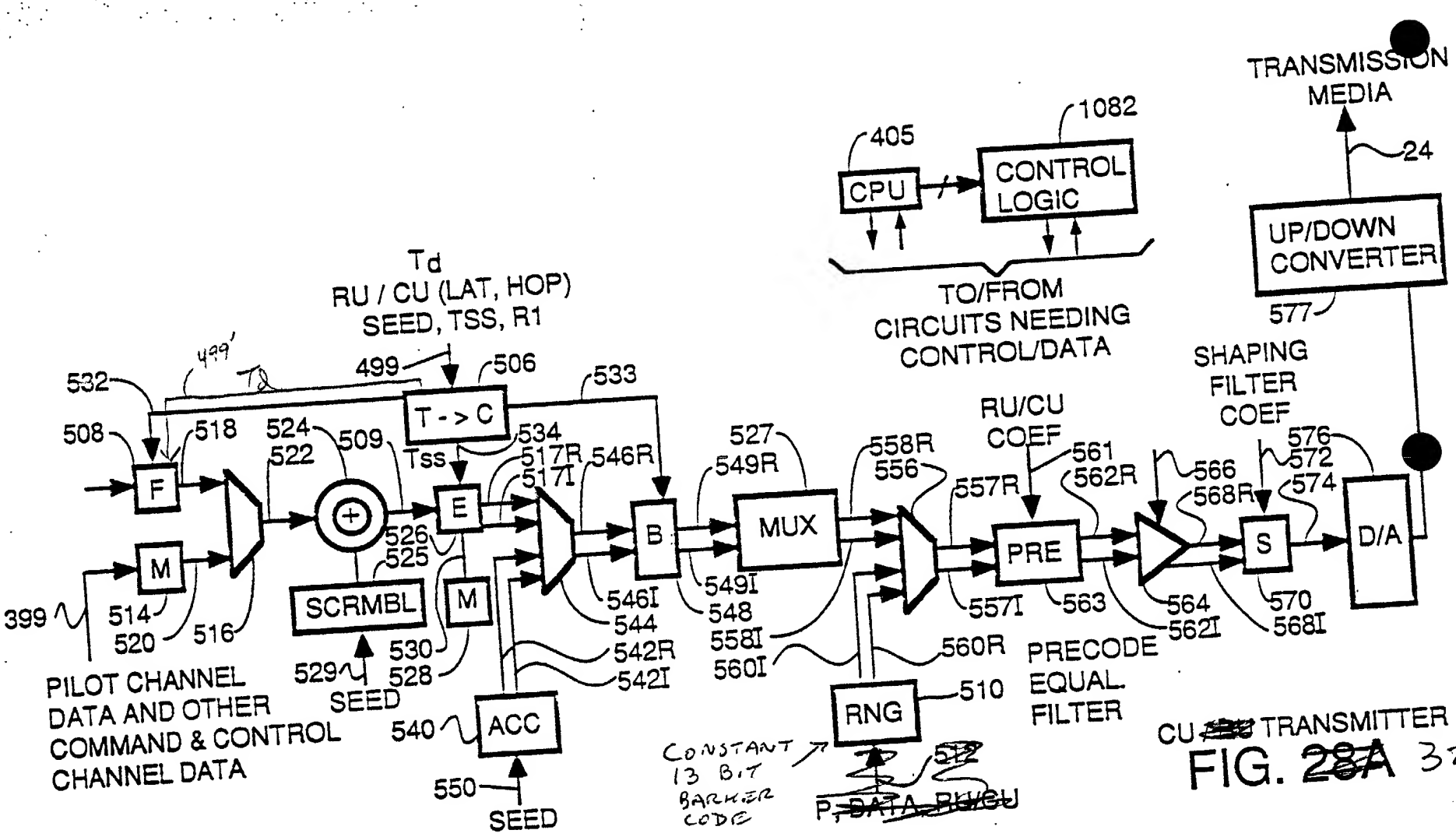

TRANSMISSION MEDIA
24
1082
405
CPU
CONTROL LOGIC
UP/DOWN CONVERTER
577
TO/FROM CIRCUITS NEEDING CONTROL/DATA
Td
RU / CU (LAT, HOP) SEED, TSS, R1
499'
499
506
533
532
508
518
524
522
509
T -> C
534
Tss
517R
517I
546R
527
549R
RU/CU COEF
558R
556
561
562R
557R
566
568R
576
572
574
SHAPING FILTER COEF
F
E
B
MUX
PRE
S
D/A
526
525
M
399
514
520
516
SCRMBL
M
546I
544
549I
548
558I
560I
557I
563
564
562I
570
568I
PILOT CHANNEL DATA AND OTHER COMMAND & CONTROL CHANNEL DATA
529
SEED
530
528
542R
542I
560R
PRECODE EQUAL FILTER
RNG
510
540
ACC
550
SEED
CONSTANT 13 BIT BARKER CODE
P-DATA RU/CU
CU TRANSMITTER

FIG. 28A

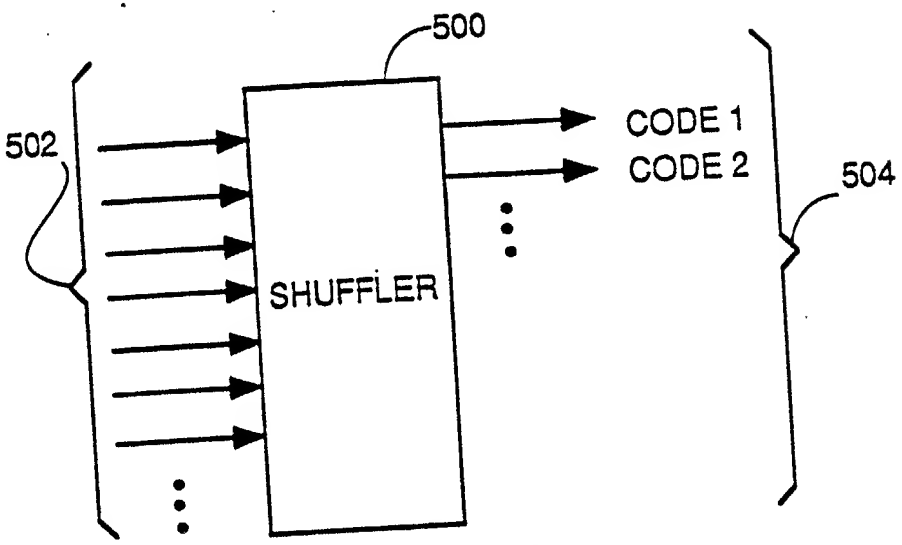


FIG. 27 38

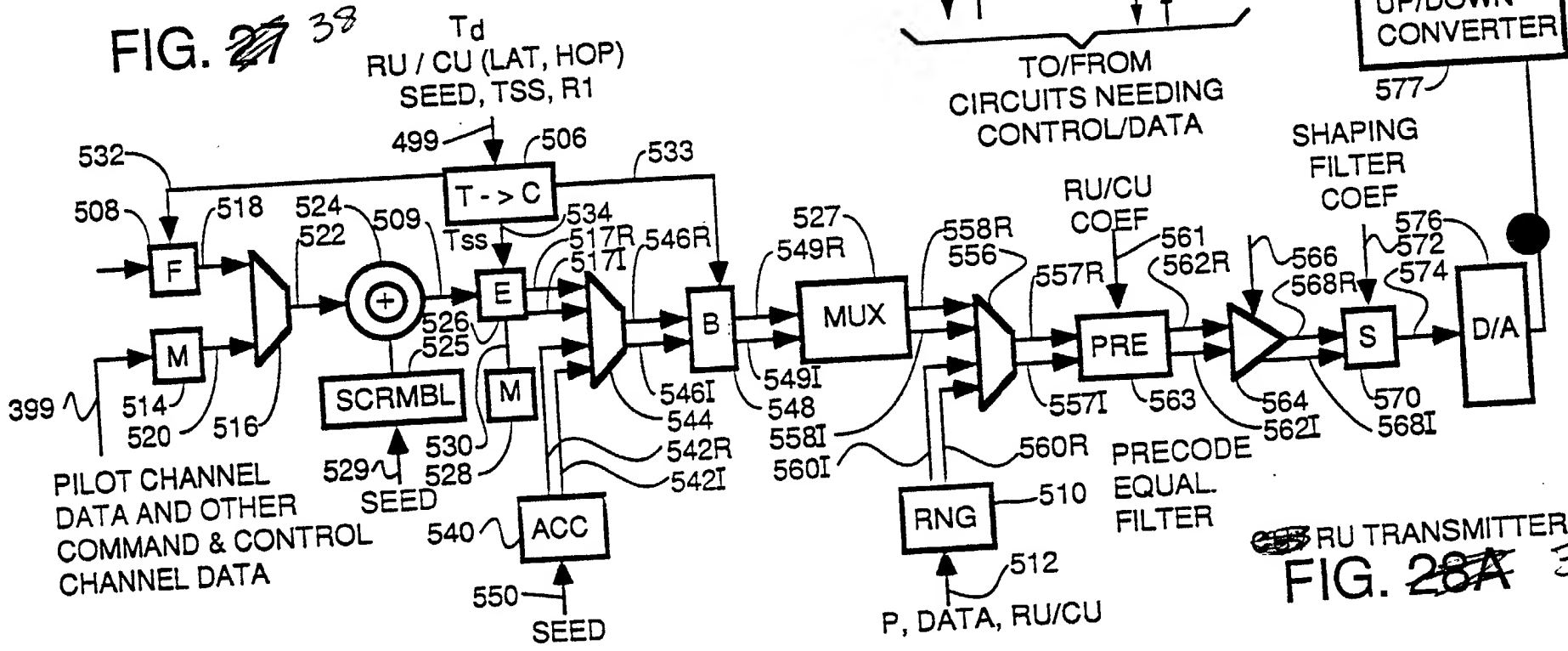


FIG. 28A

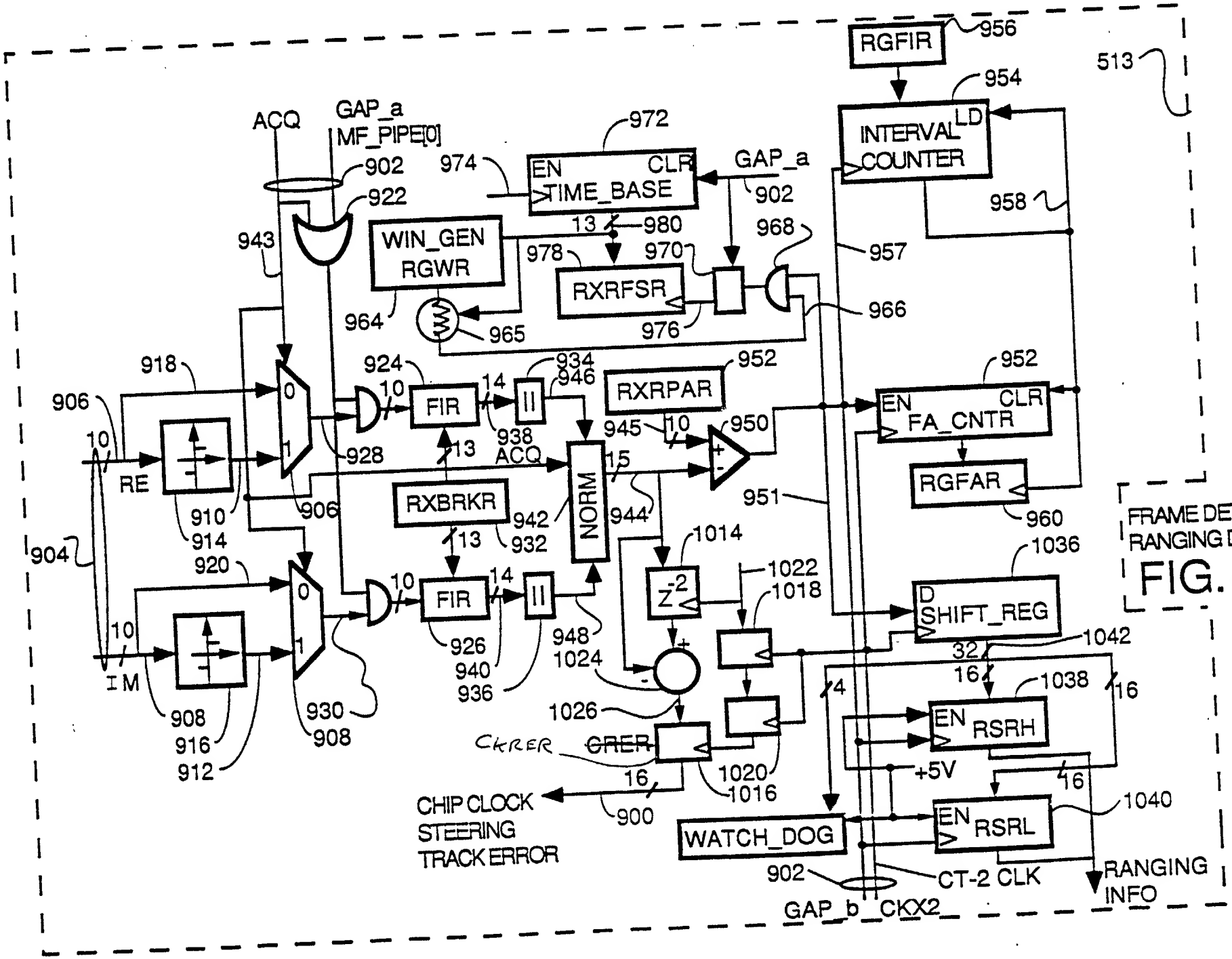

RGFIR
956
513
954
INTERVAL COUNTER
LD
ACQ
GAP_a
MF_PIPE[0]
902
922
974
EN
CLR
TIME_BASE
972
GAP_a
902
958
943
WIN_GEN
RGWR
13
980
968
978
970
RXRFSR
957
964
965
976
966
924
934
946
952
RXRPAR
952
906
10
14
FIR
II
EN
CLR
FA_CNTR
938
945
10
950
928
13
ACQ
15
RE
910
914
RXBRKR
942
932
NORM
944
951
RGFAR
960
904
13
1014
1036
920
1022
1018
10
14
FIR
II
Z-2
D
SHIFT_REG
10
926
940
936
948
1024
1042
32
16
1038
16
IM
908
916
912
930
908
1026
4
EN
RSRH
CKRER
GRER
1020
1016
+5V
16
16
CHIP CLOCK
STEERING
TRACK ERROR
900
WATCH_DOG
EN
RSRL
1040
902
CT-2 CLK
RANGING
INFO
GAP_b
CKX2
FRAME DETECTOR/
RANGING DETECTOR

FIG. 38

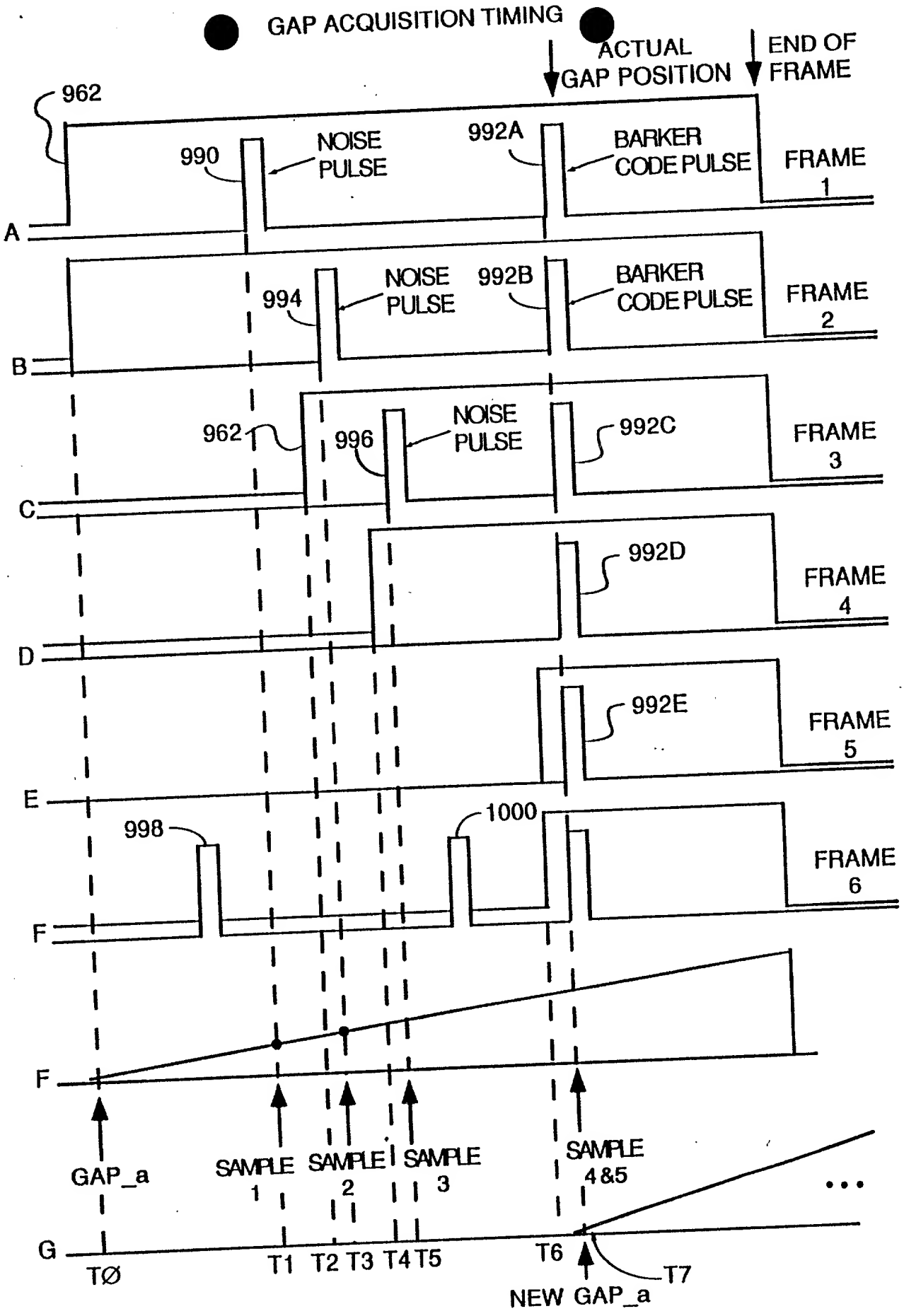
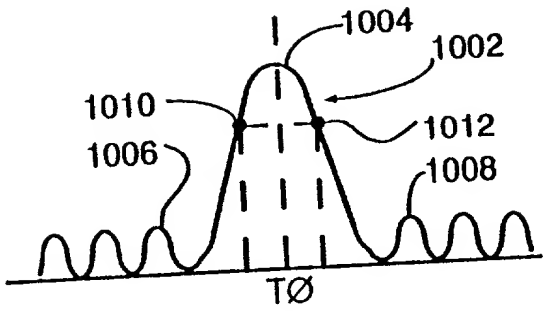
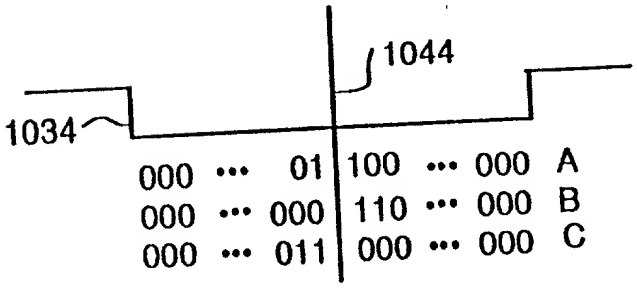

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
...
G
TØ
T1 T2 T3 T4 T5
T6
T7
NEW GAP_a

FIG. 39 35



36

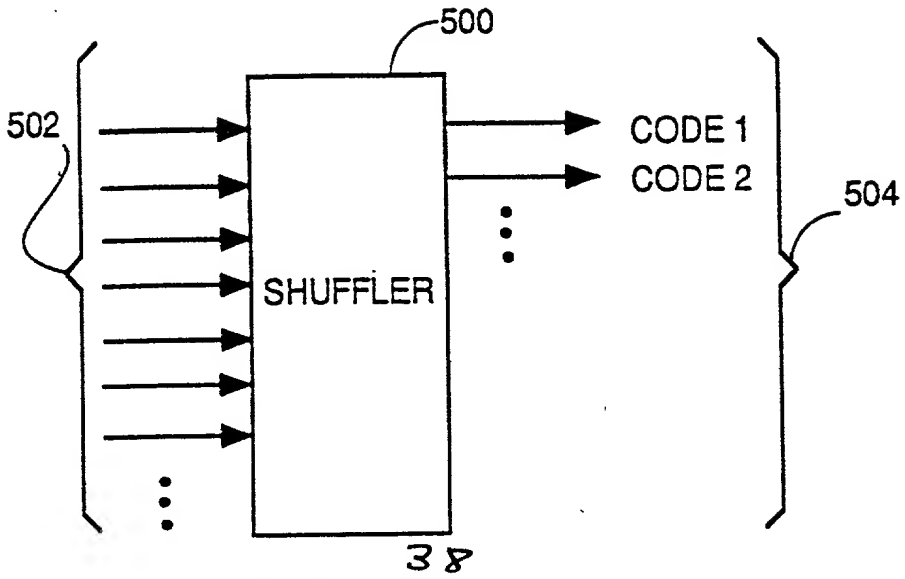
FIG. ~~40~~



37

FIG. ~~41~~

FINE TUNING TO CENTER BARMER CODE



38

FIG. 27

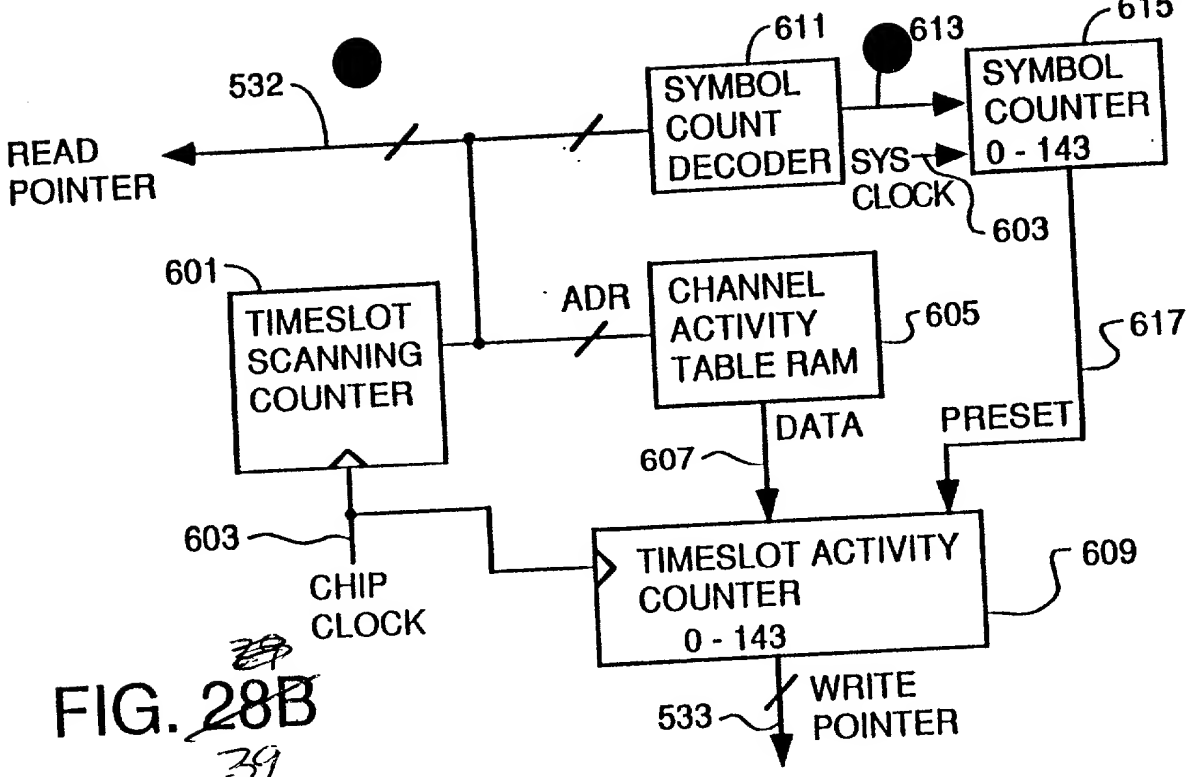


FIG. 28B

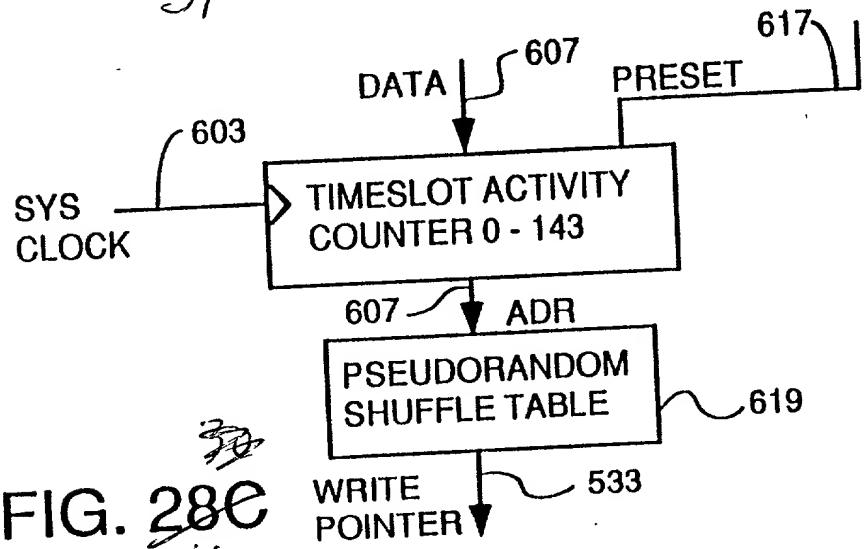


FIG. 28C

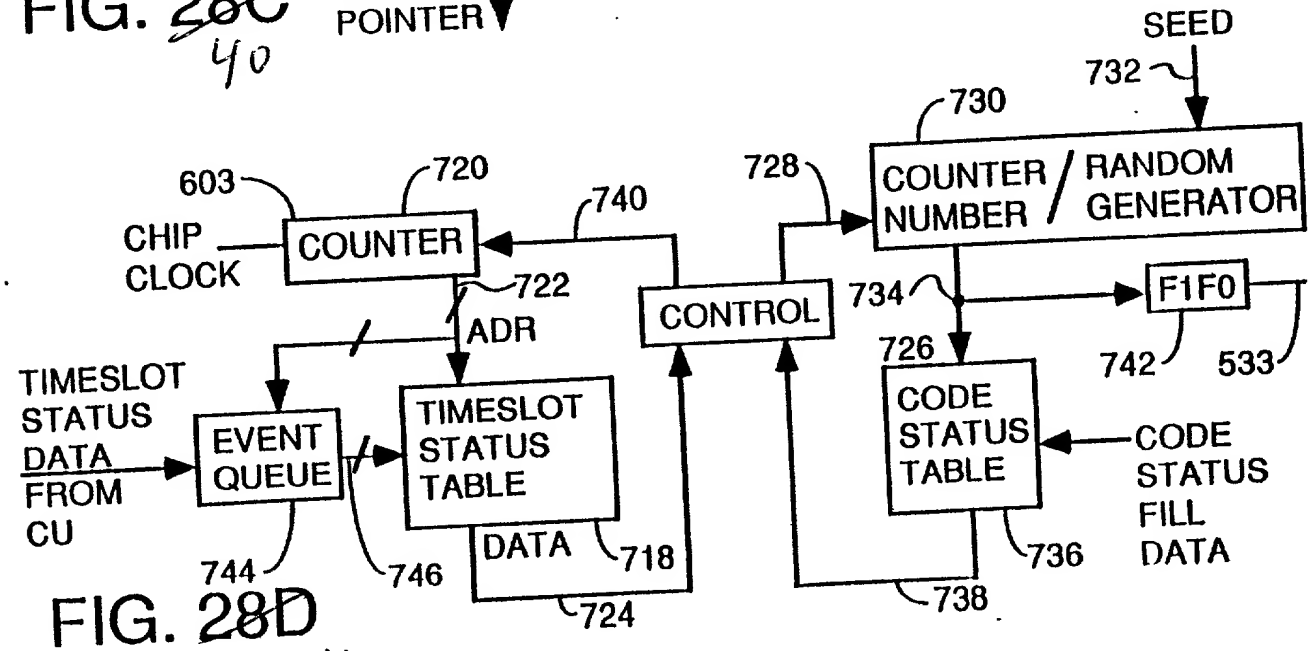
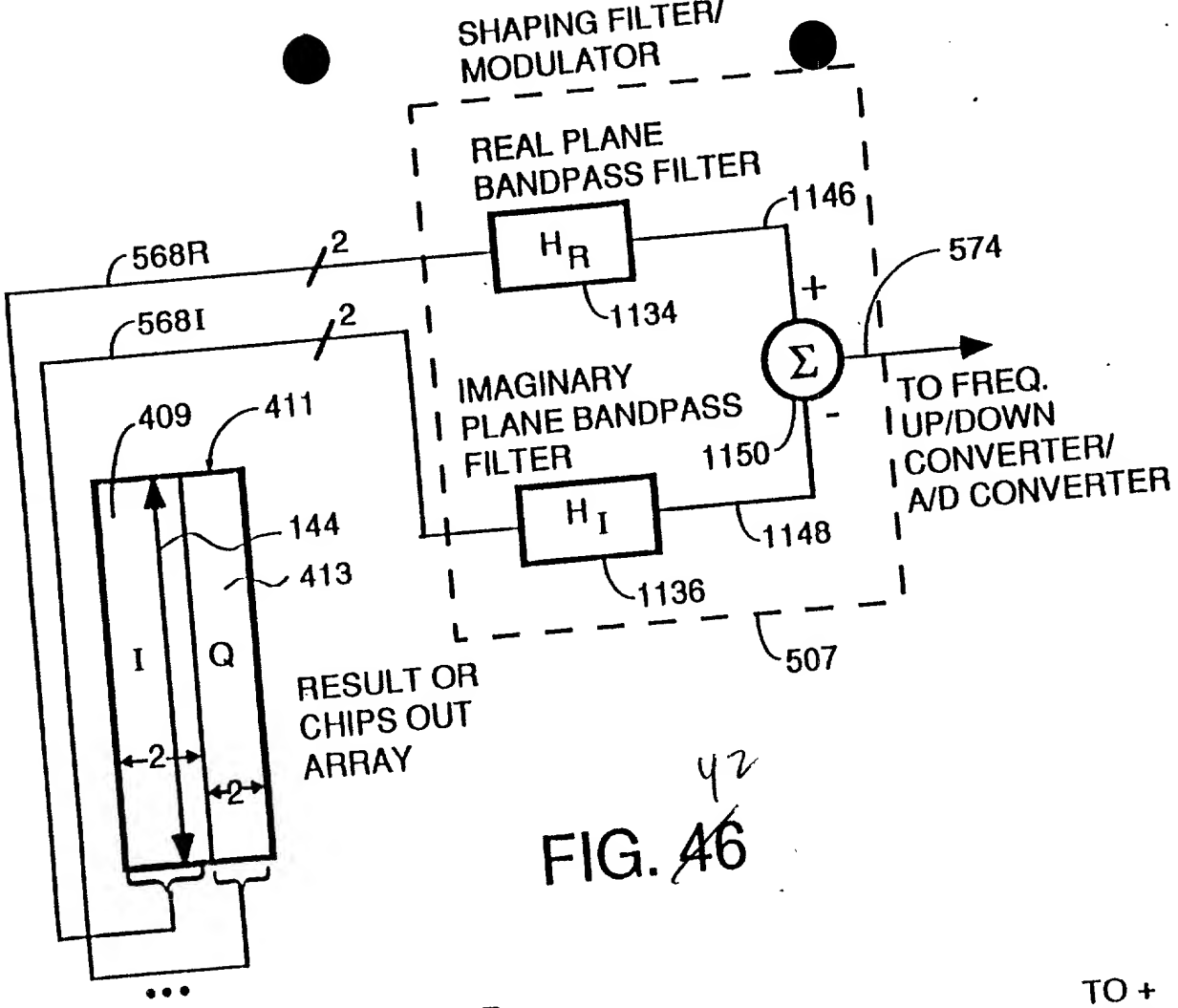
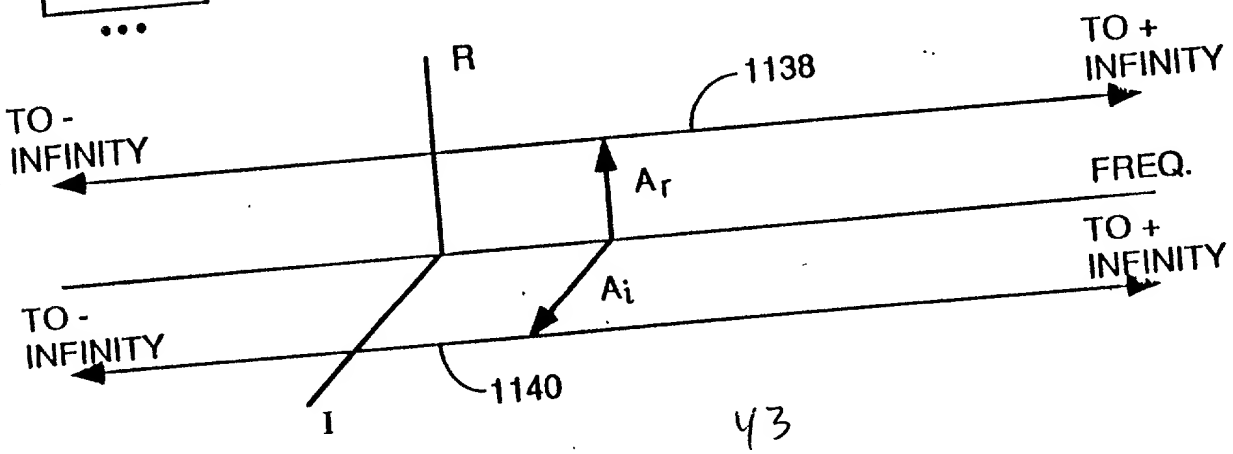


FIG. 28D



42

FIG. 46



43

FIG. 47

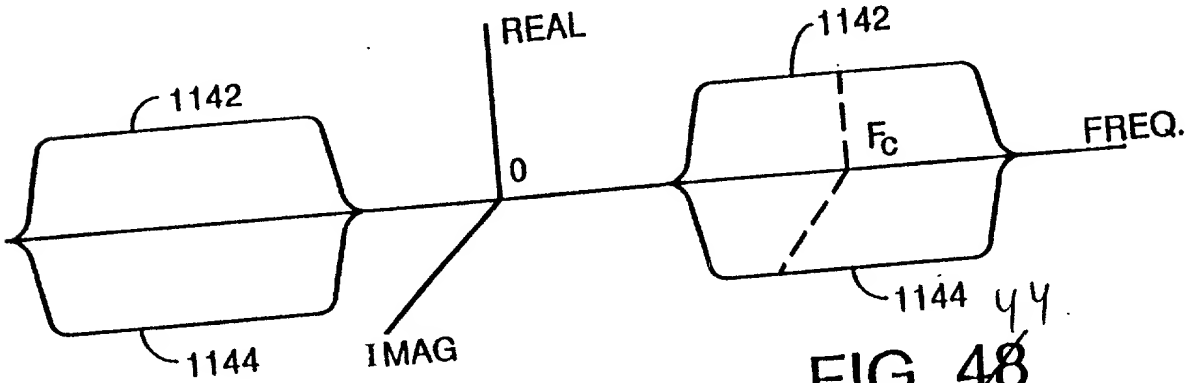
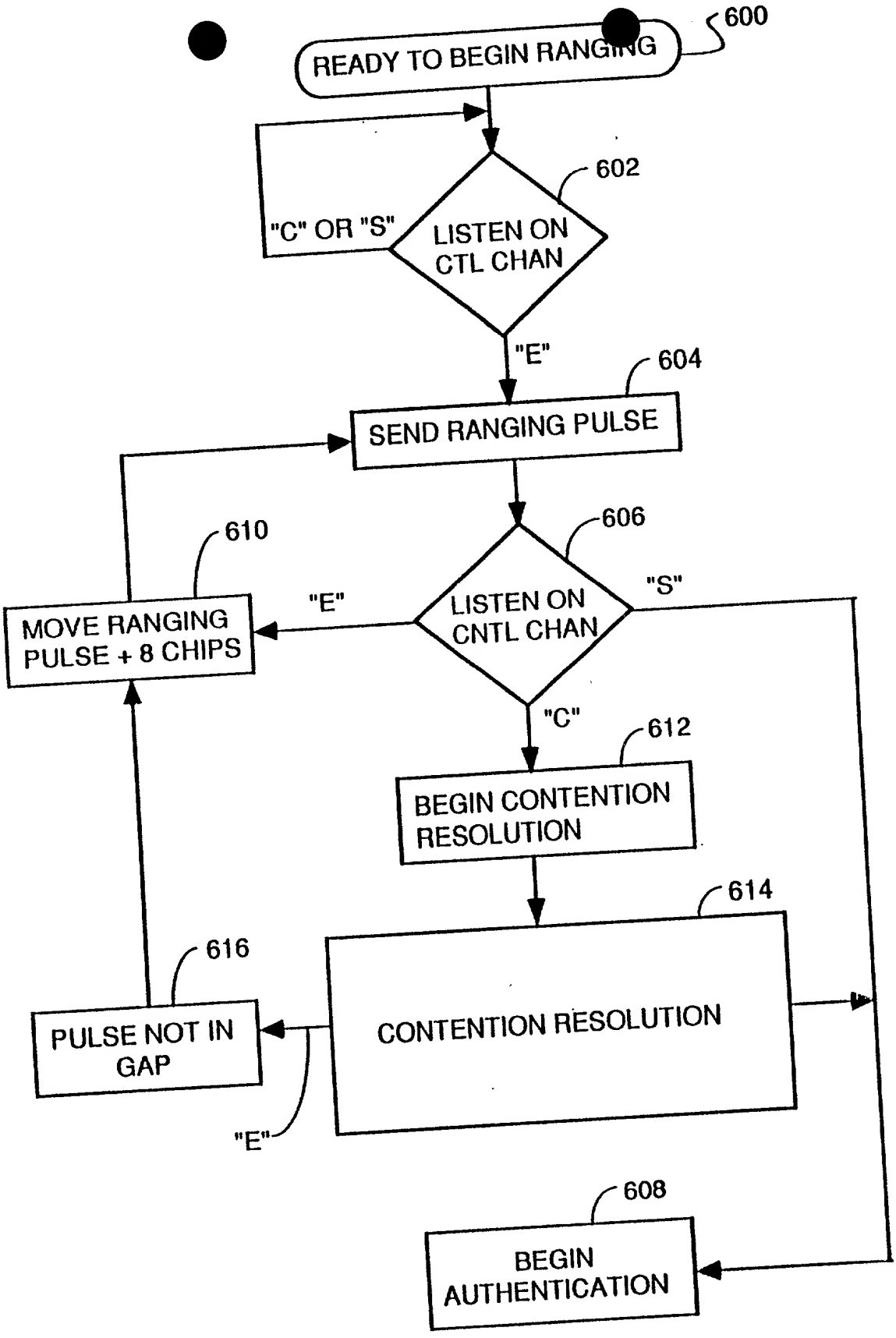
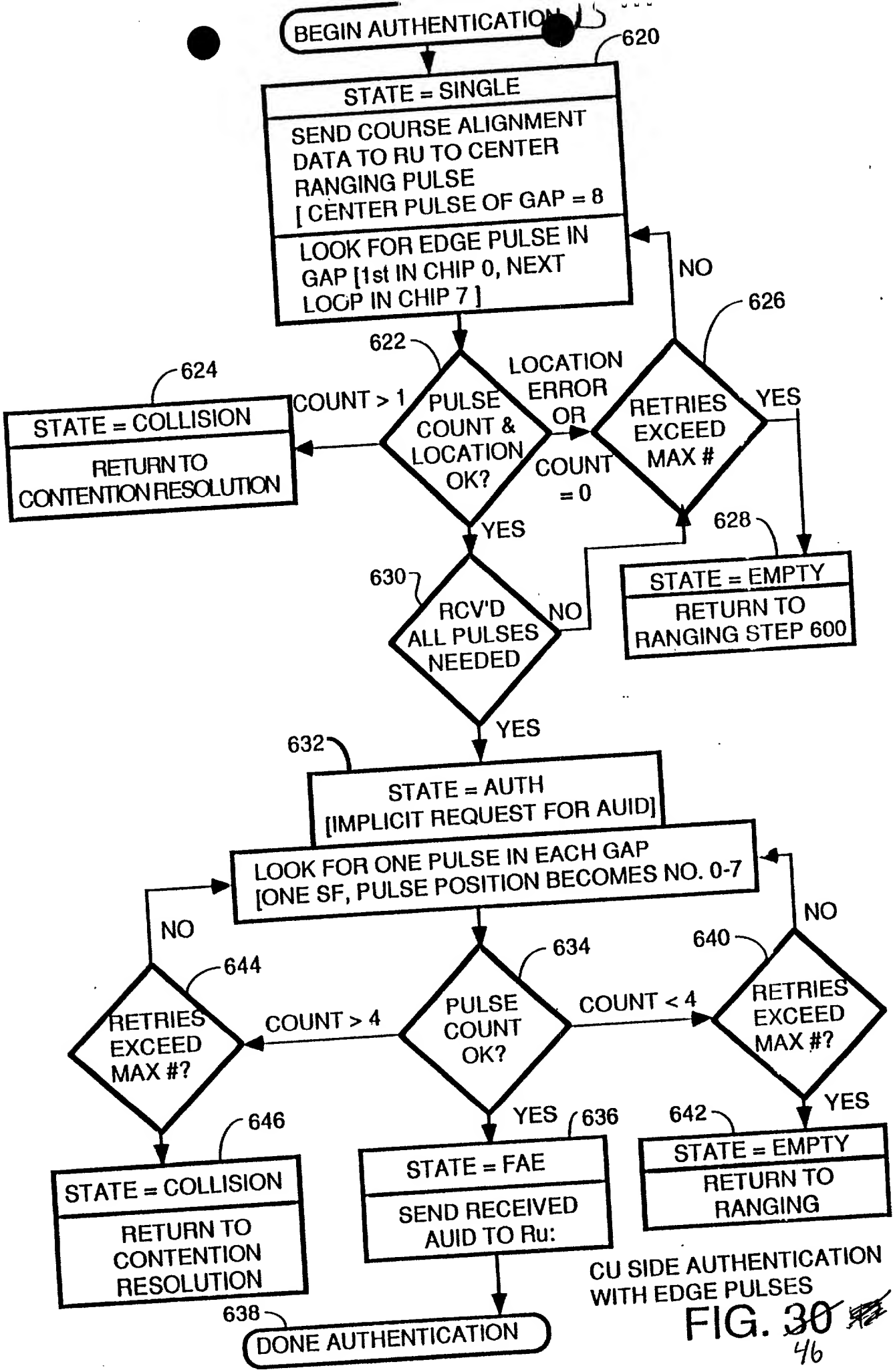


FIG. 48



RU RANGING

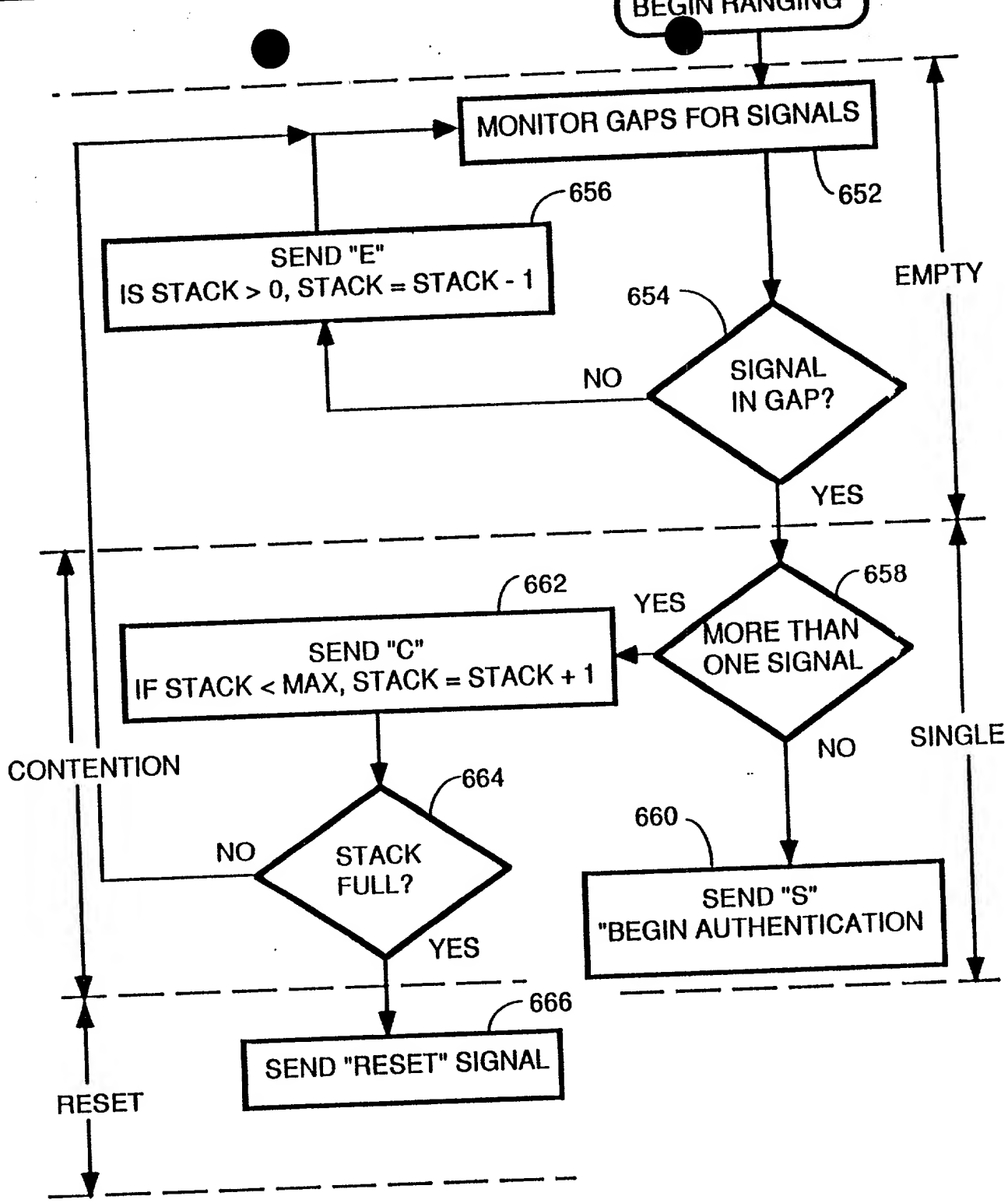
FIG. 29



CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 30

46

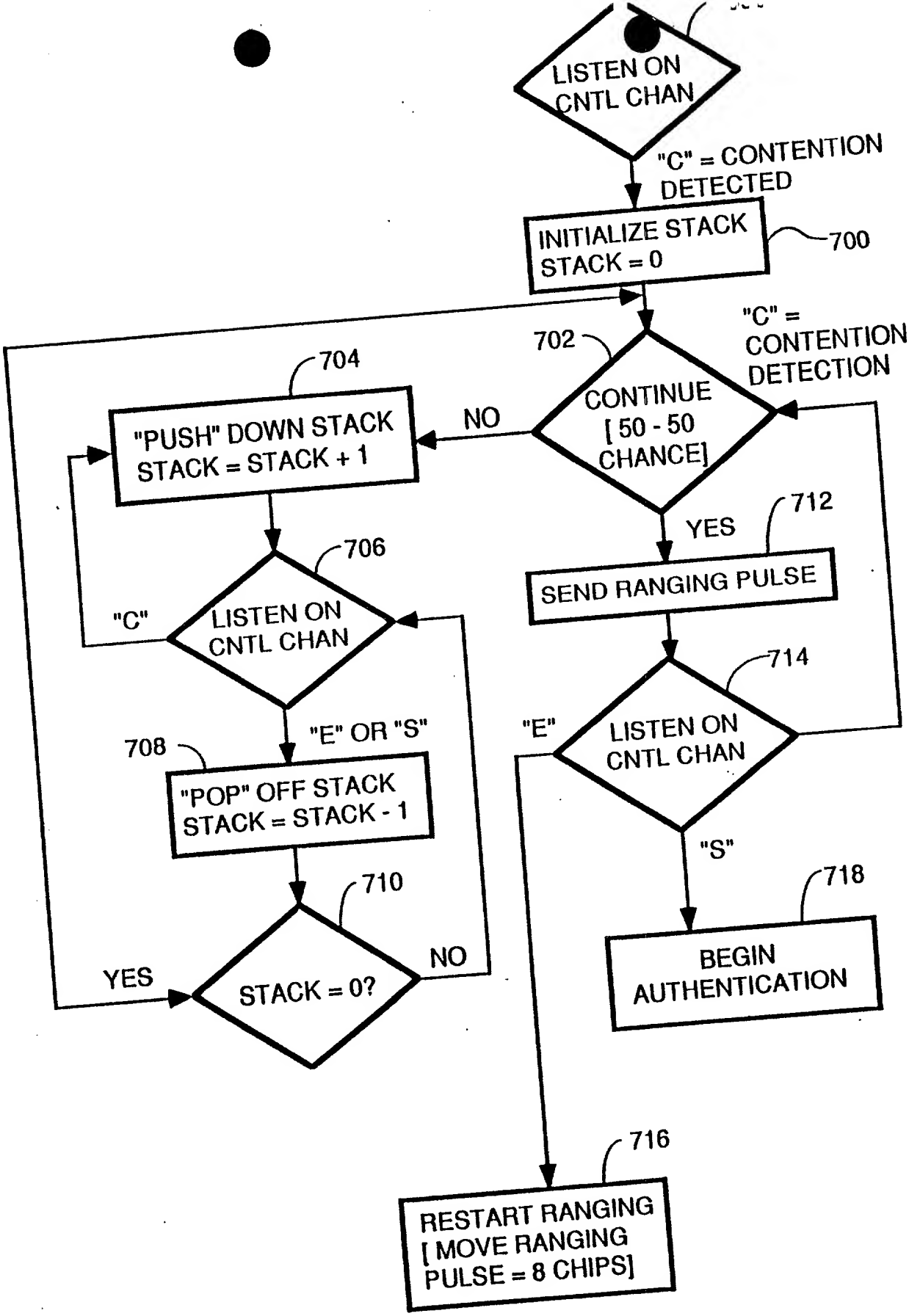


CU RANGING & CONTENTION RESOLUTION

~~RANGING AND CONTENTION RESOLUTION~~
~~CU SIDE~~

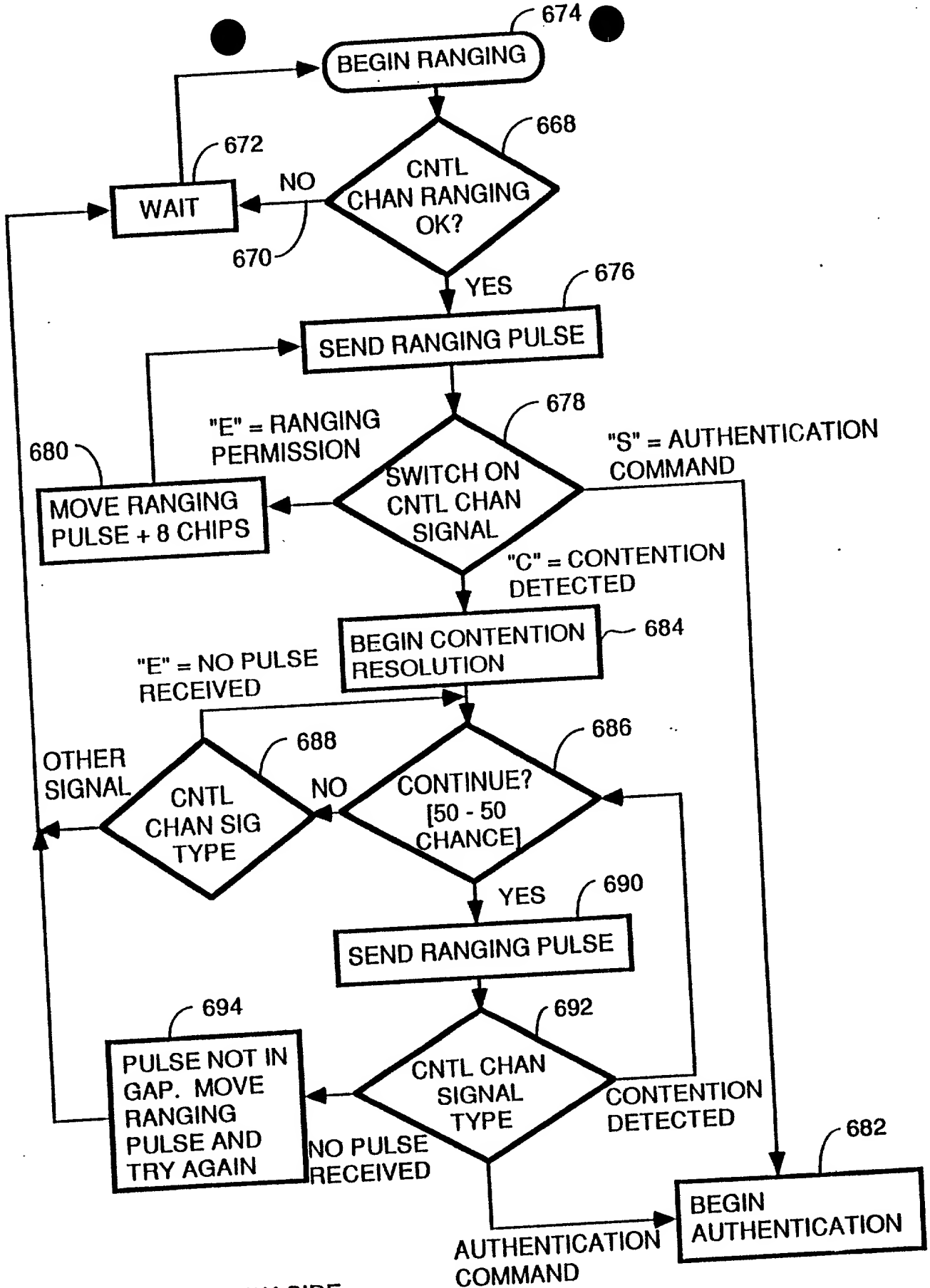
FIG. 31

41



CONTENTION RESOLUTION - RU
USING BINARY STACK

FIG. 33



RANGING - RU SIDE
BINARY TREE
ALGORITHM

FIG. 32

50
49

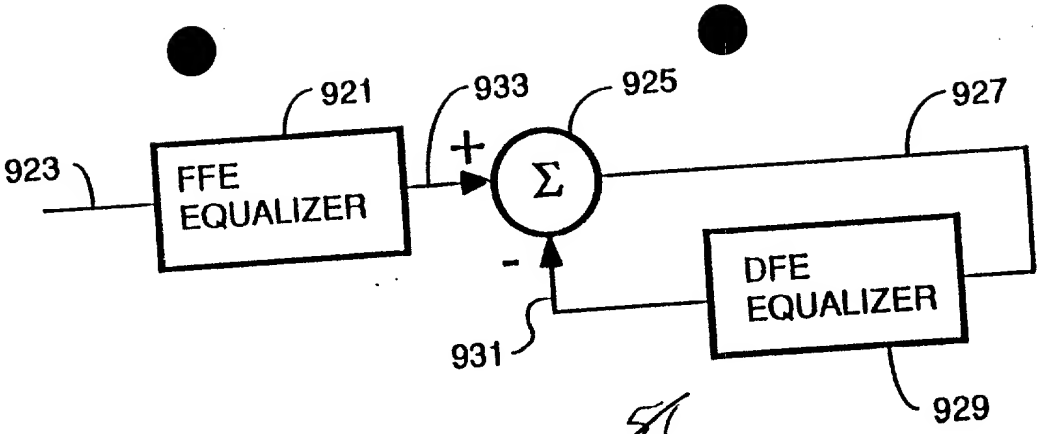


FIG. 37

50

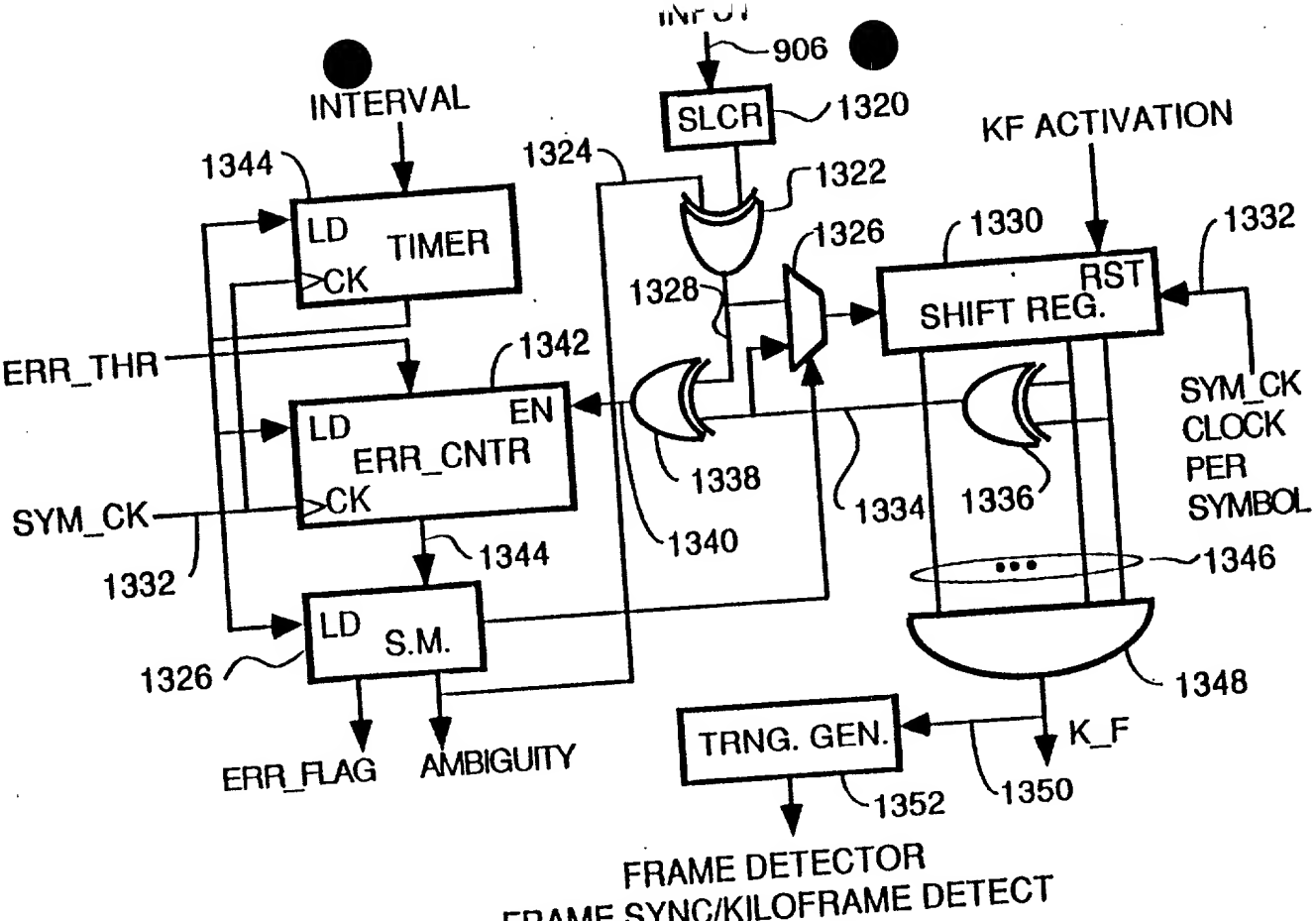
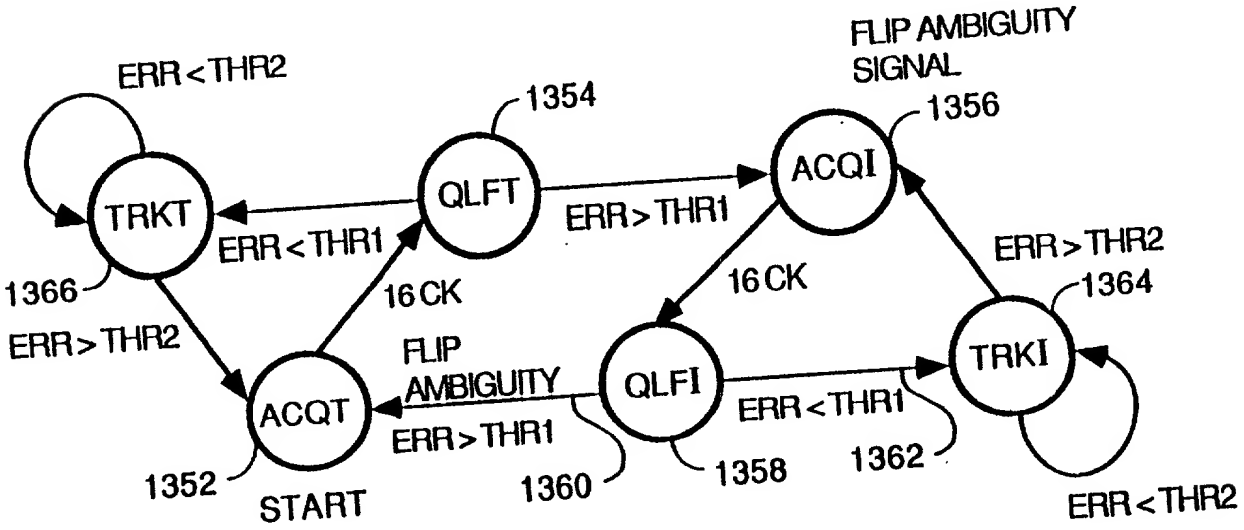


FIG. 52

51



STATE MACHINE

FIG. 53

52

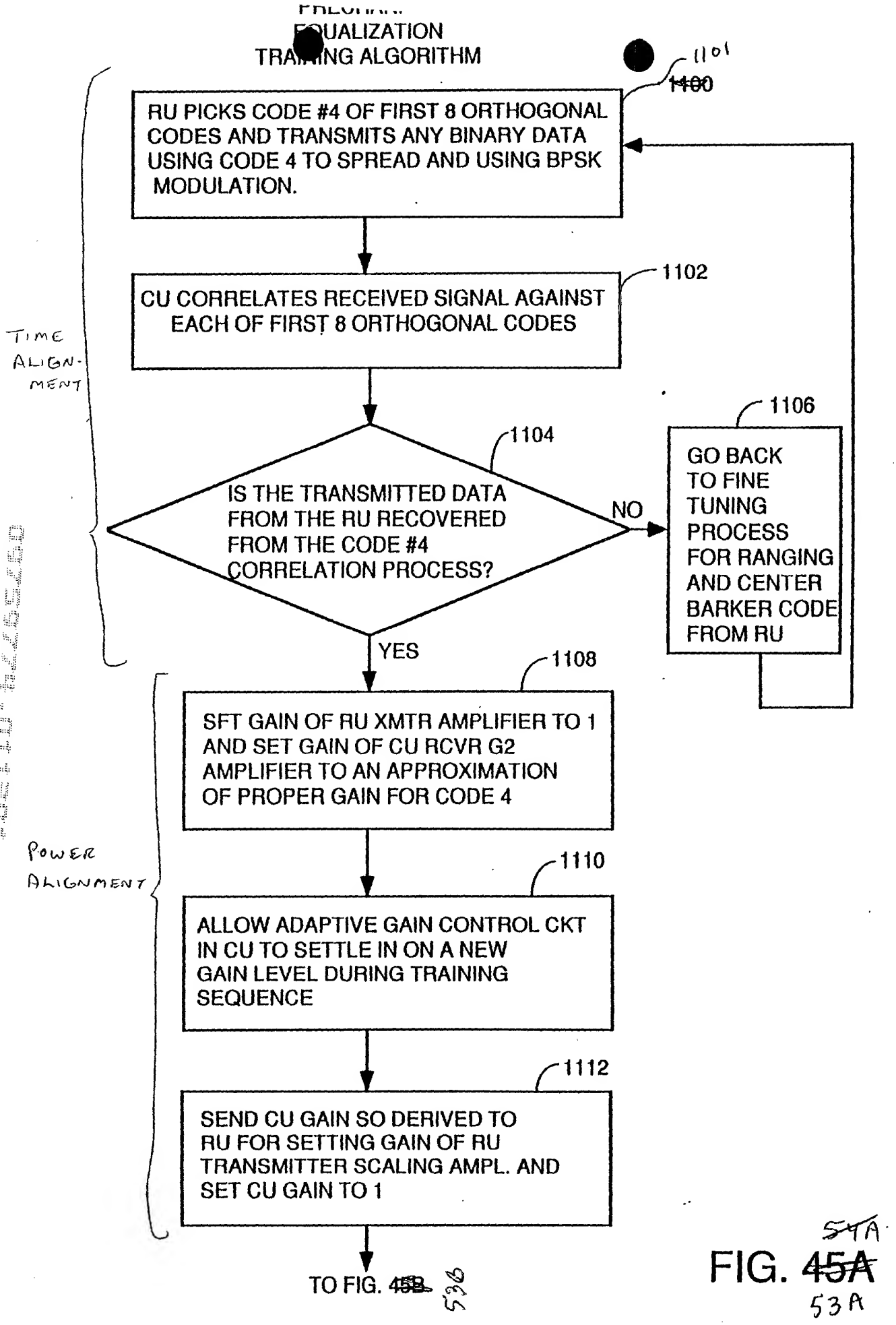


FIG. 45A
54A
53A

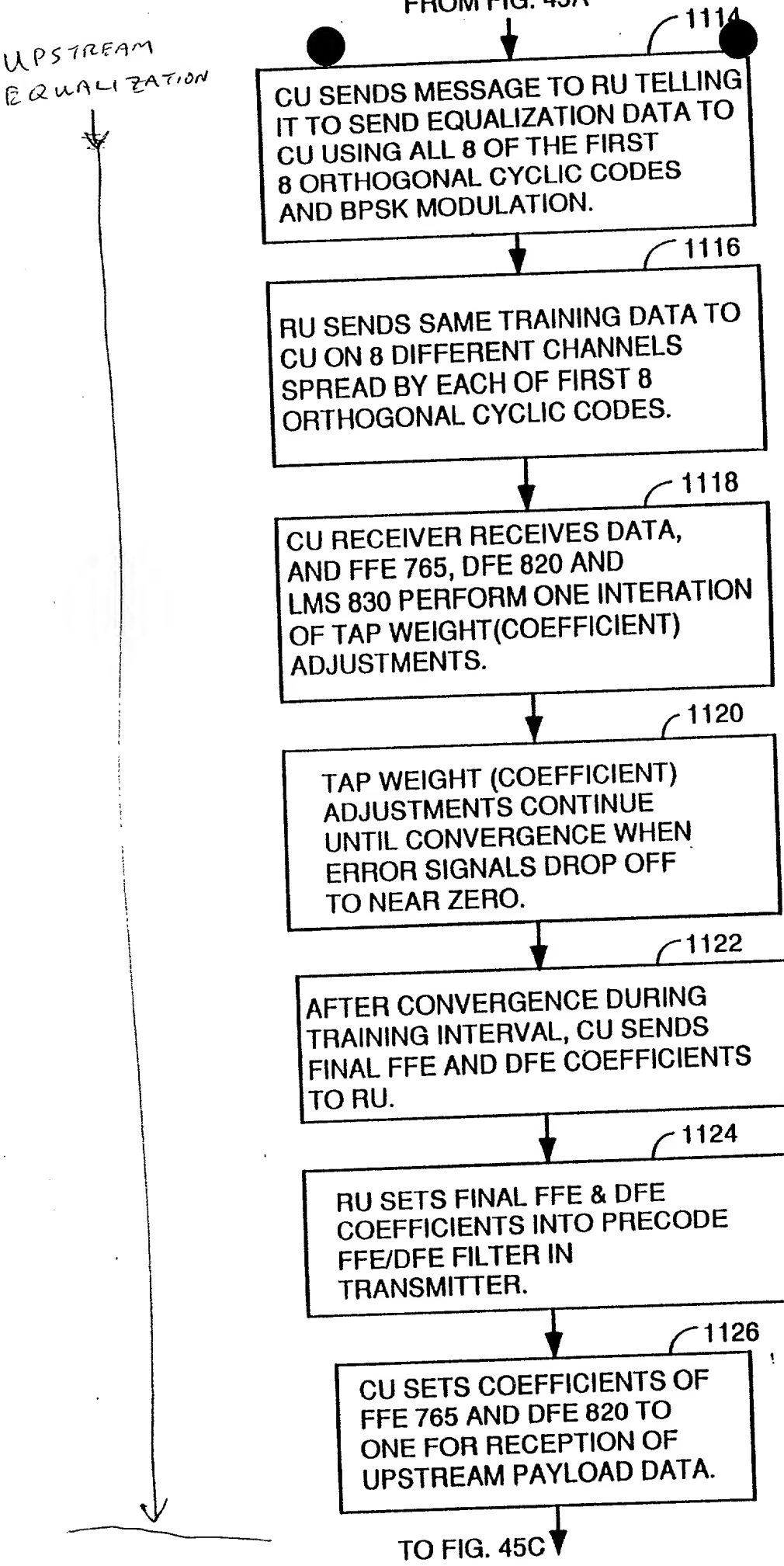


FIG. ~~45B~~ 53B
~~53B~~
53B

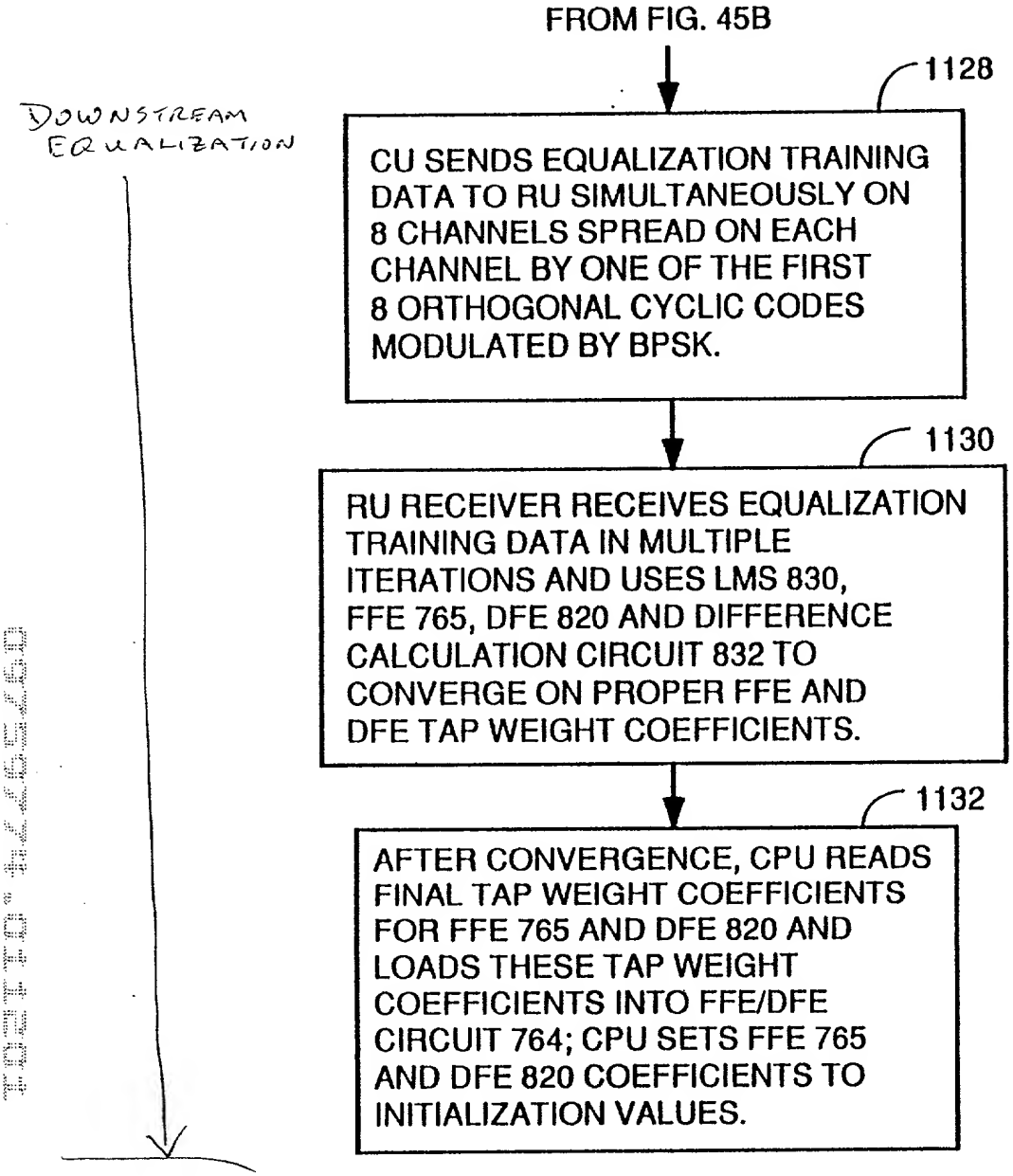


FIG. 45C

54C

53C

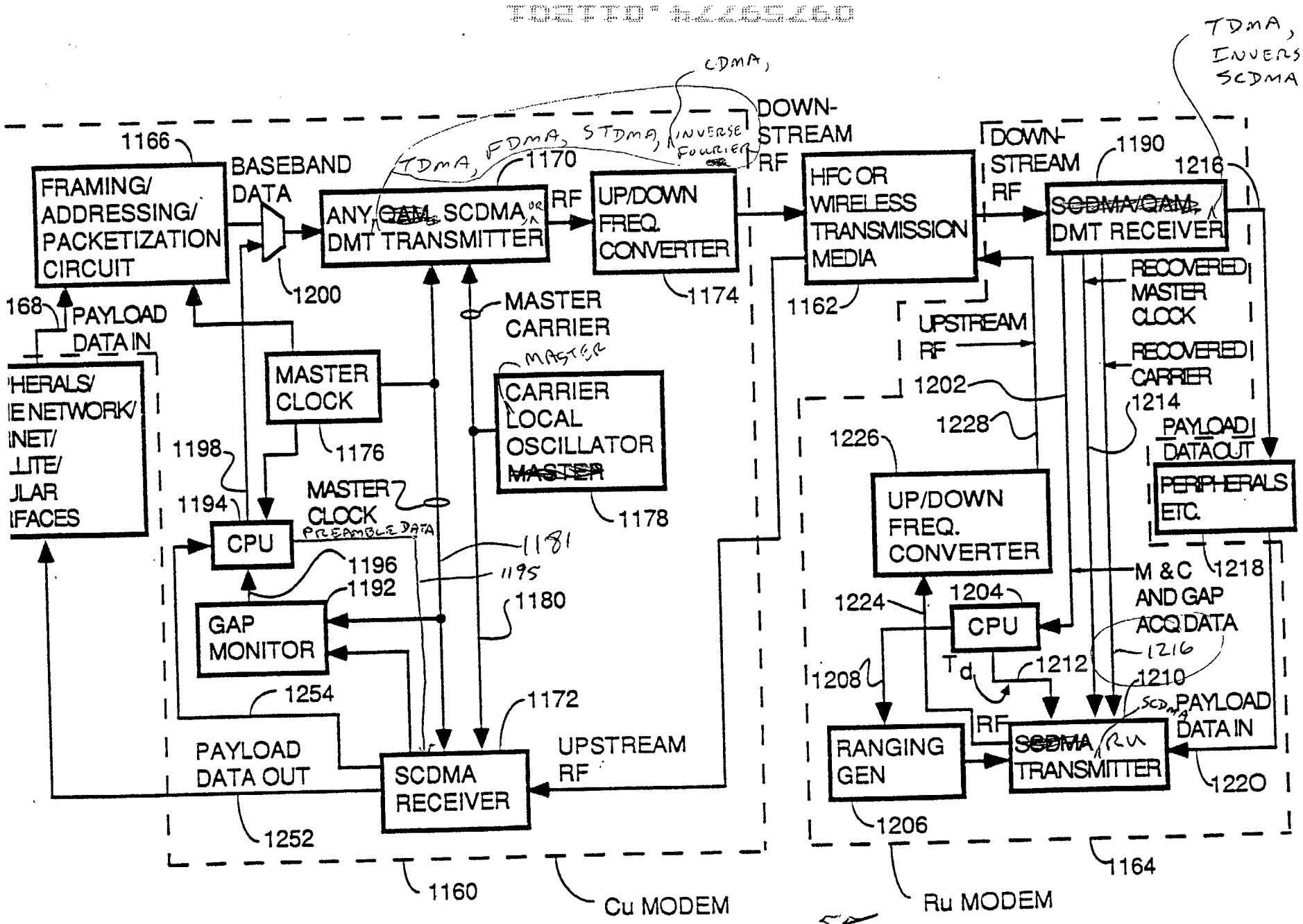
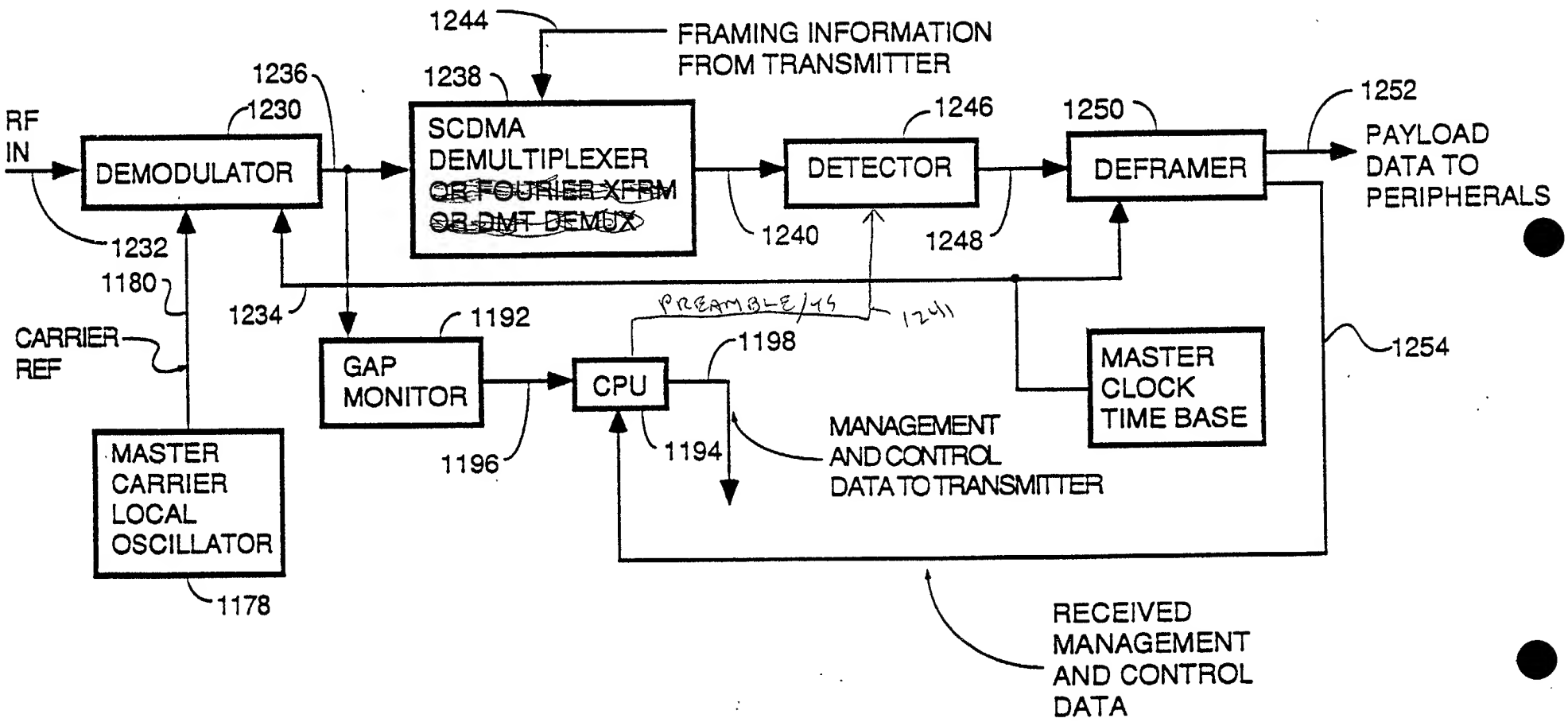

1166
FRAMING/ ADDRESSING/ PACKETIZATION CIRCUIT
BASEBAND DATA
1200
168
PAYLOAD DATA IN
HERALS/ E NETWORK/ INET/ LITE/ JLAR IFACES
MASTER CLOCK
1176
1198
1194
CPU
MASTER CLOCK
PREAMBLE DATA
1196
1192
GAP MONITOR
1254
PAYLOAD DATA OUT
1252
1160
Cu MODEM
ANY, CDMA, SCDMA, OR DMT TRANSMITTER
1170
RF
UP/DOWN FREQ. CONVERTER
1174
MASTER CARRIER
CARRIER LOCAL OSCILLATOR MASTER
1178
1181
1195
1180
1172
SCDMA RECEIVER
UPSTREAM RF
DOWN-STREAM RF
HFC OR WIRELESS TRANSMISSION MEDIA
1162
UPSTREAM RF
1202
1228
1226
UP/DOWN FREQ. CONVERTER
1224
1204
CPU
1208
Td
1212
1210
RANGING GEN
1206
RF
SCDMA TRANSMITTER
1220
1164
Ru MODEM
DOWN-STREAM RF
1190
1216
SCDMA/CDMA DMT RECEIVER
RECOVERED MASTER CLOCK
RECOVERED CARRIER
1214
PAYLOAD DATA OUT
PERIPHERALS ETC.
1218
M & C AND GAP ACQ DATA
1216
SCDMA PAYLOAD DATA IN
TDMA, STDMA, F
INVERSE FOURIE
SCDMA, CDMA OR
CDMA,
TDMA, FDMA, STDMA, INVERSE FOURIER OR

FIG. 49

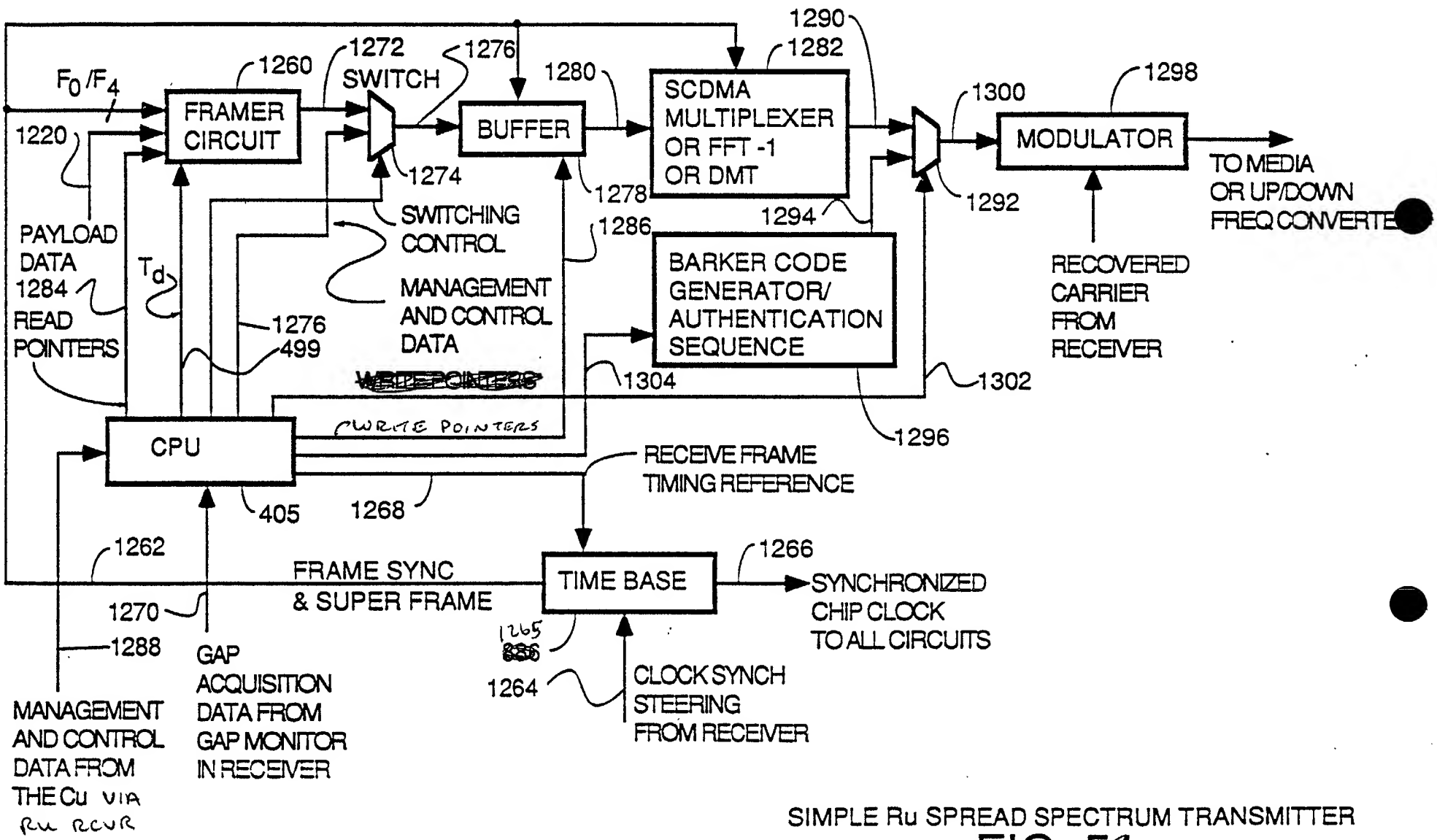
54



SIMPLE Cu SPREAD SPECTRUM RECEIVER

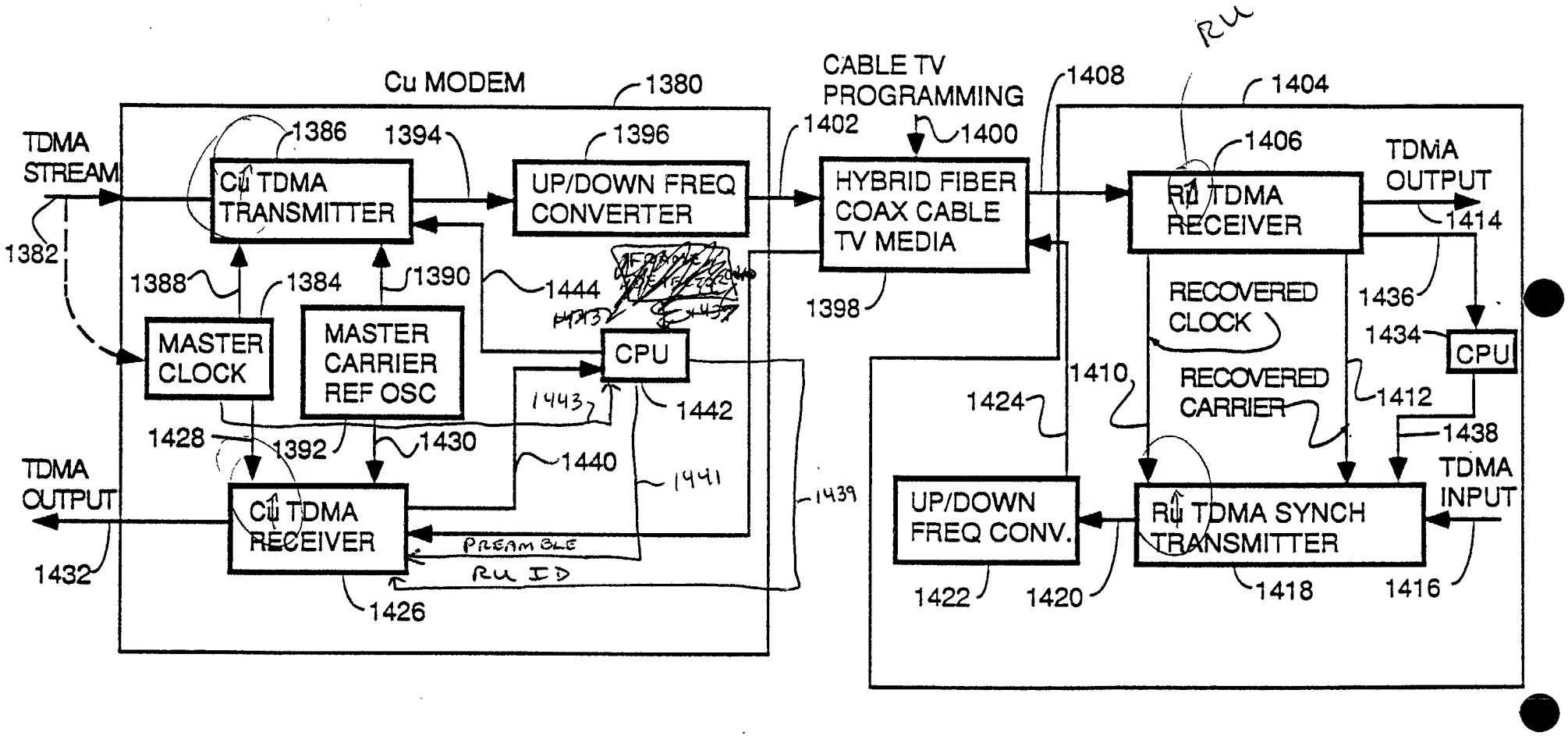
FIG. 50 56

55



SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. 5~~1~~
~~5~~
56



SYNCHRONOUS TDMA SYSTEM

FIG. 54

57

OFFSET	1B ASIC		2A ASIC	
(Chips)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

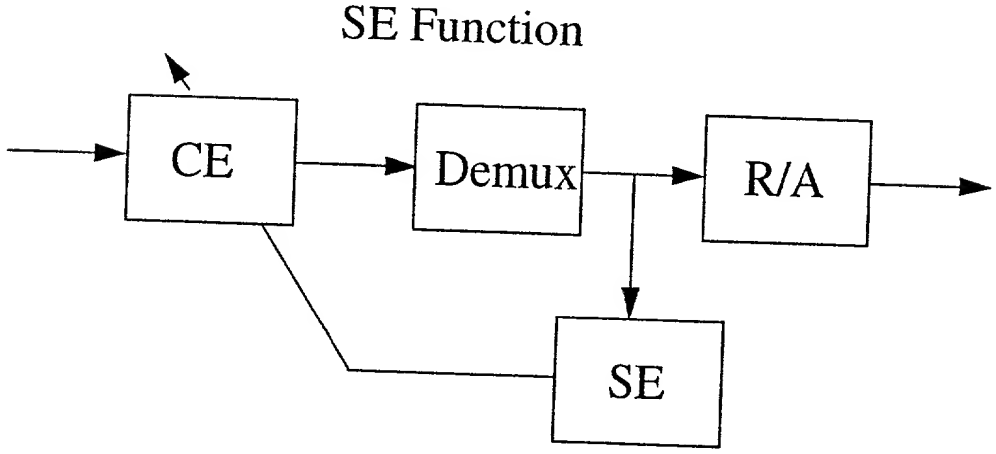
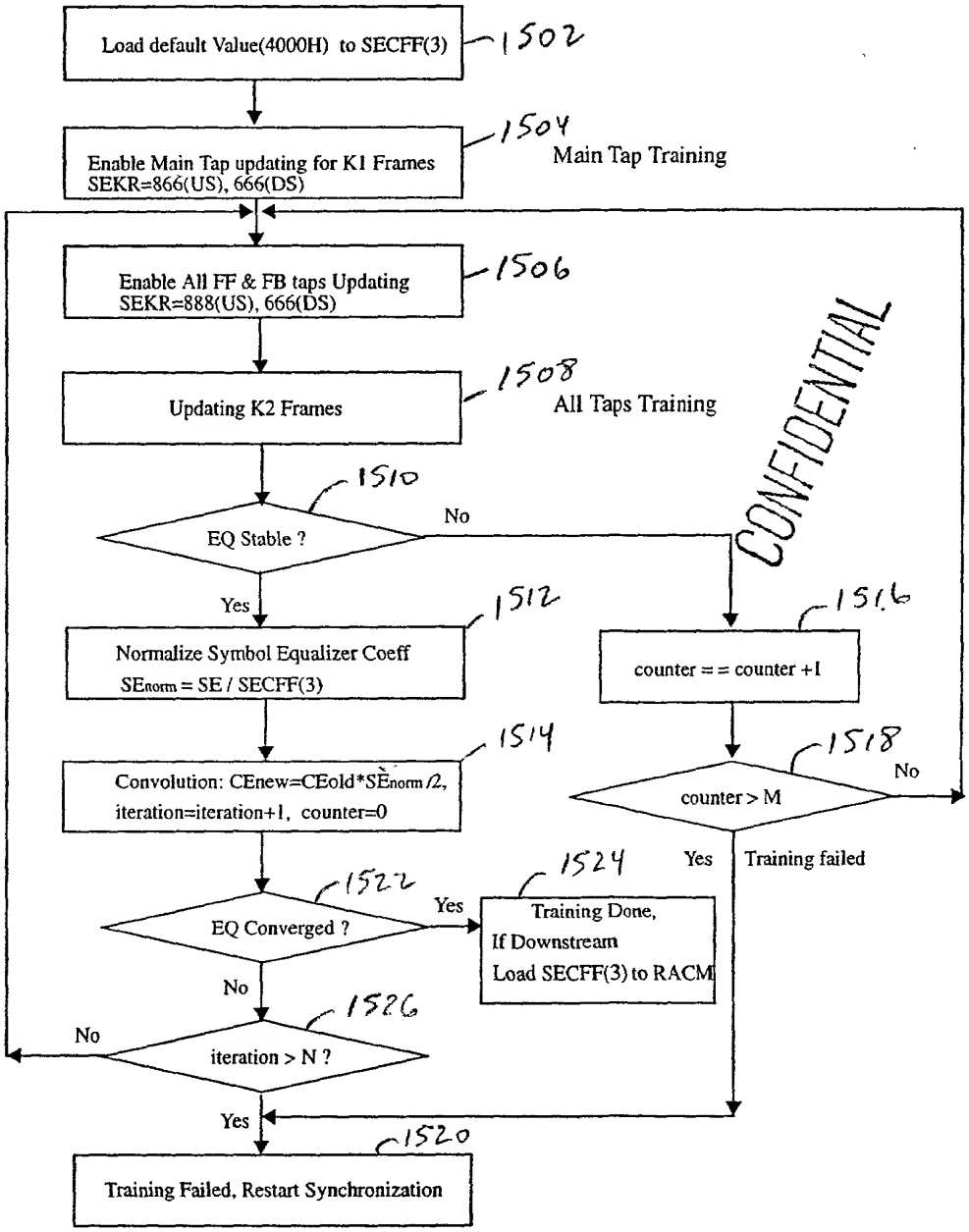


FIG. 59

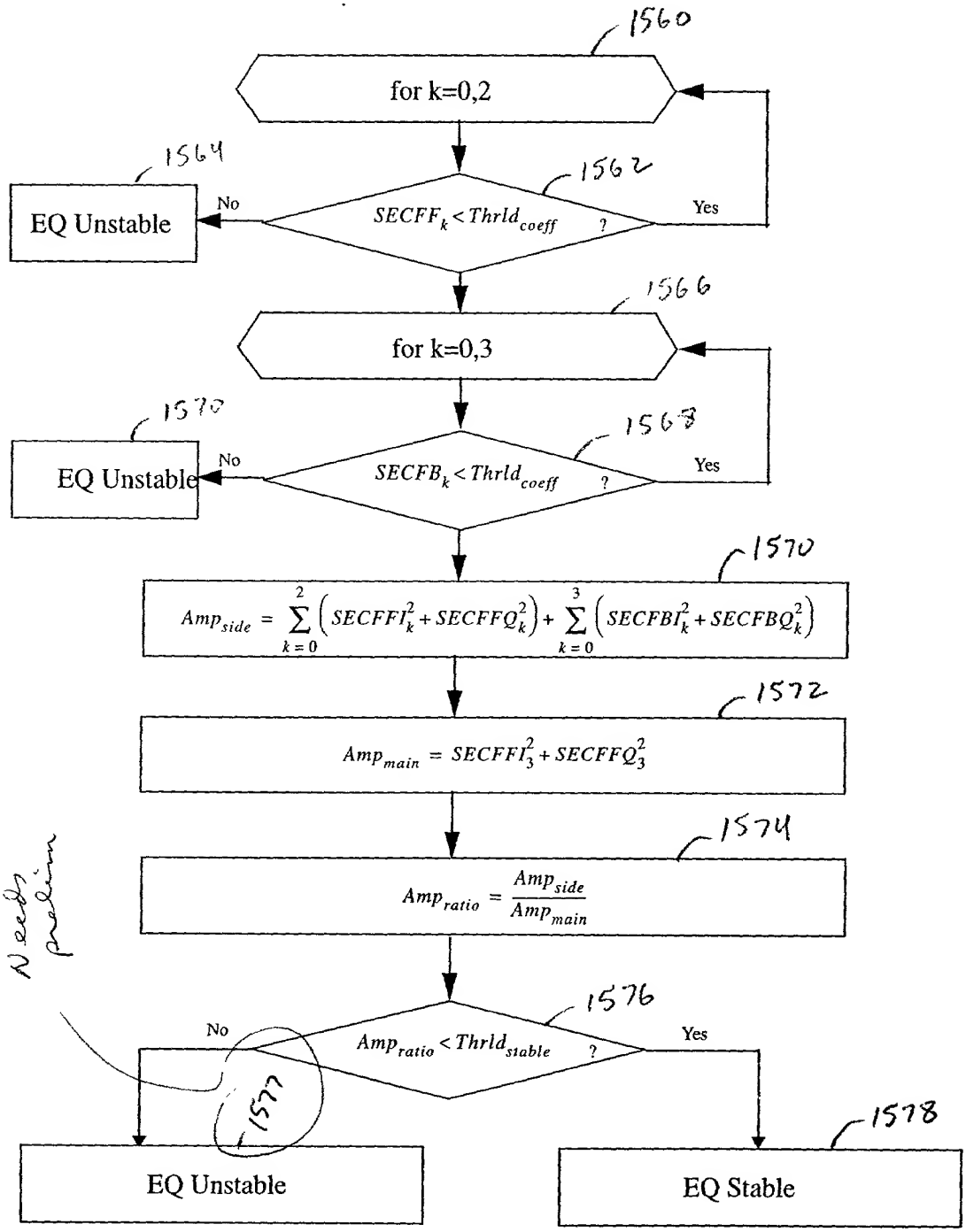
Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

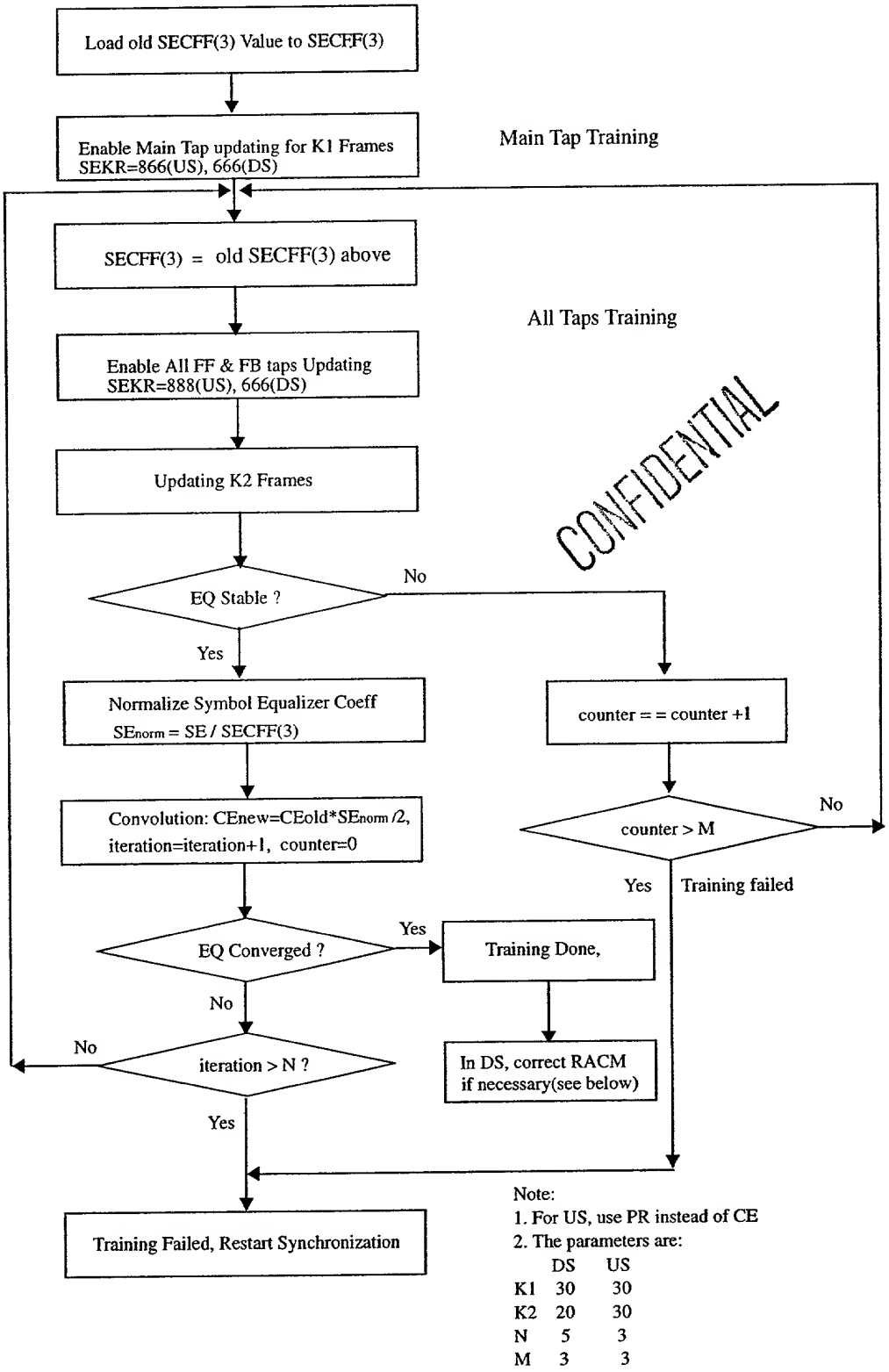
EQ Stability Check



Note: $Thrld_{coeff}$ = 7F00H $Thrld_{stable}$ = 10^{-3}

FIG. 61

Periodic 2-Step Training Algorithm

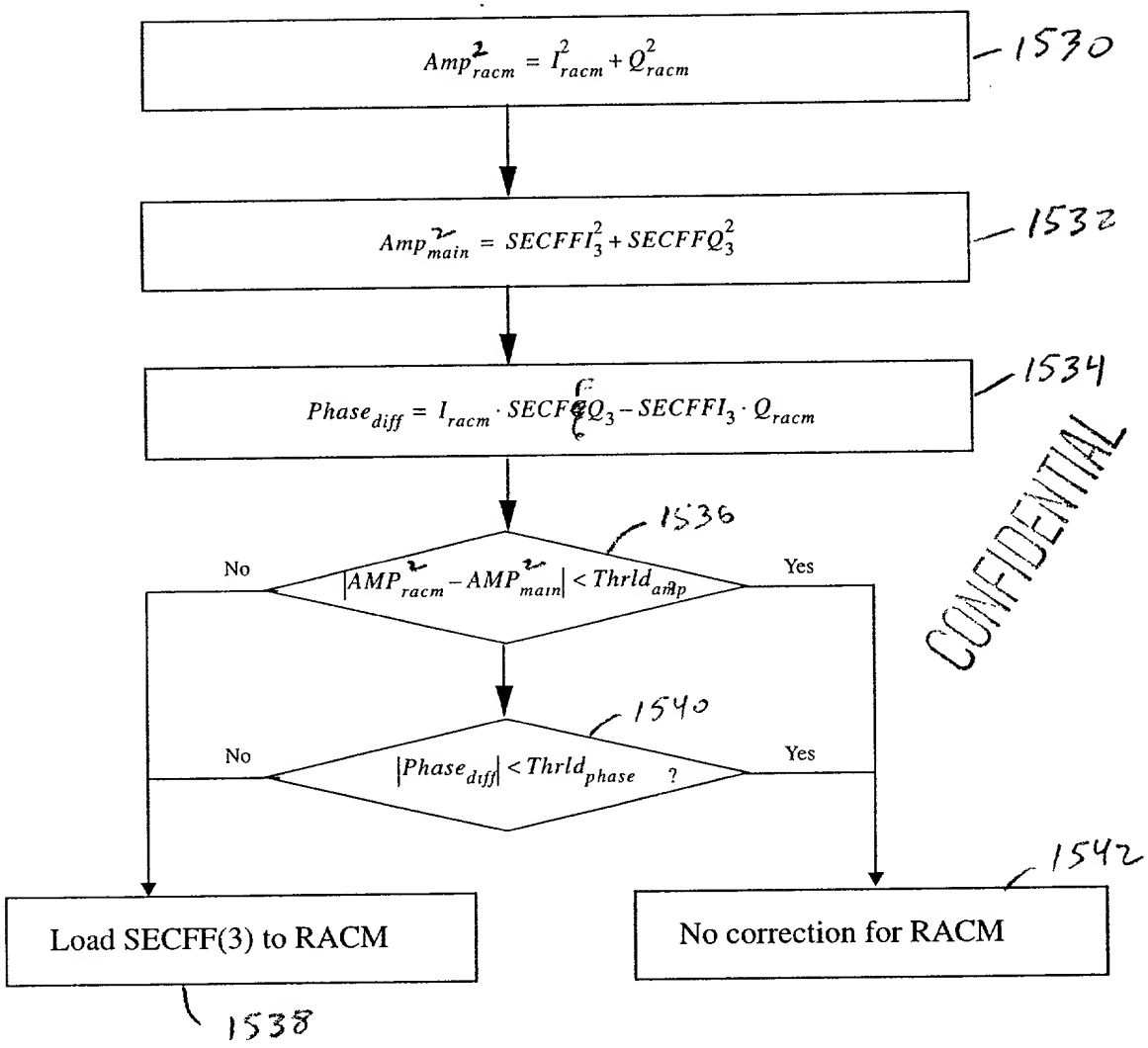


Note:
1. For US, use PR instead of CE
2. The parameters are:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM Correction



CONFIDENTIAL

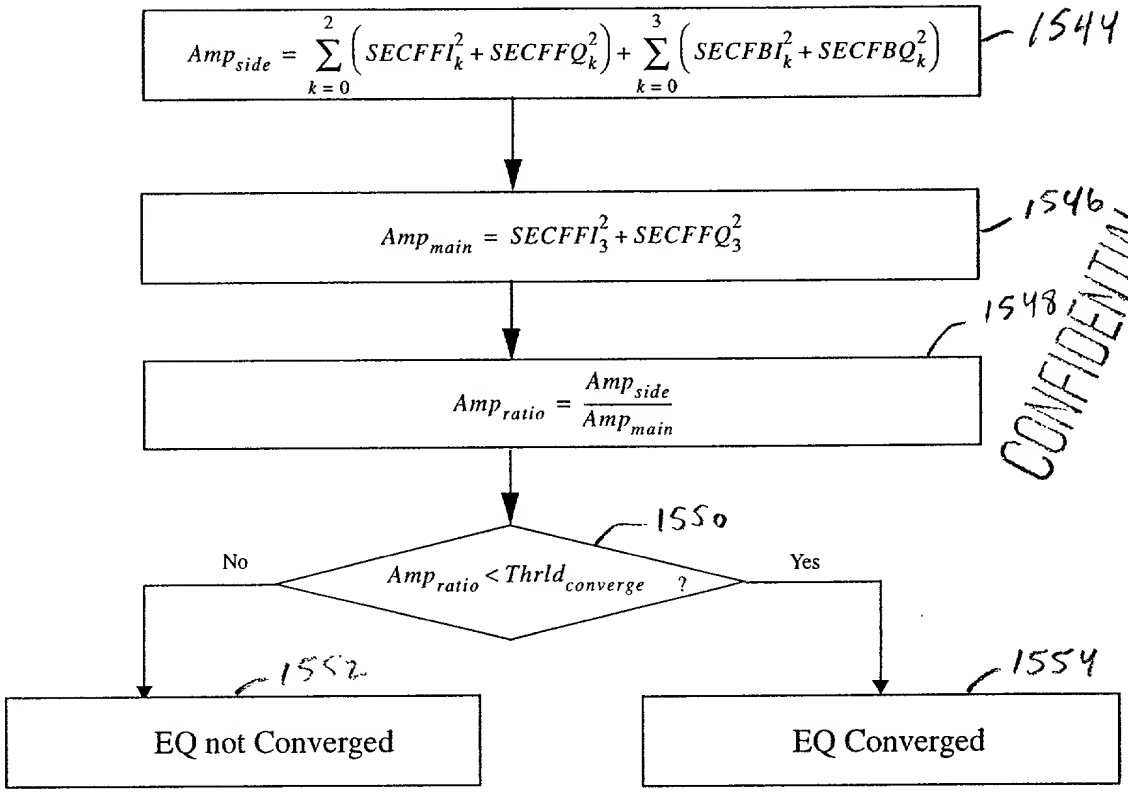
Note: $Thrld_{amp} = TBD$

$Thrld_{phase} = TBD$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

EQ Convergence Check



Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

Power Alignment Flow Chart

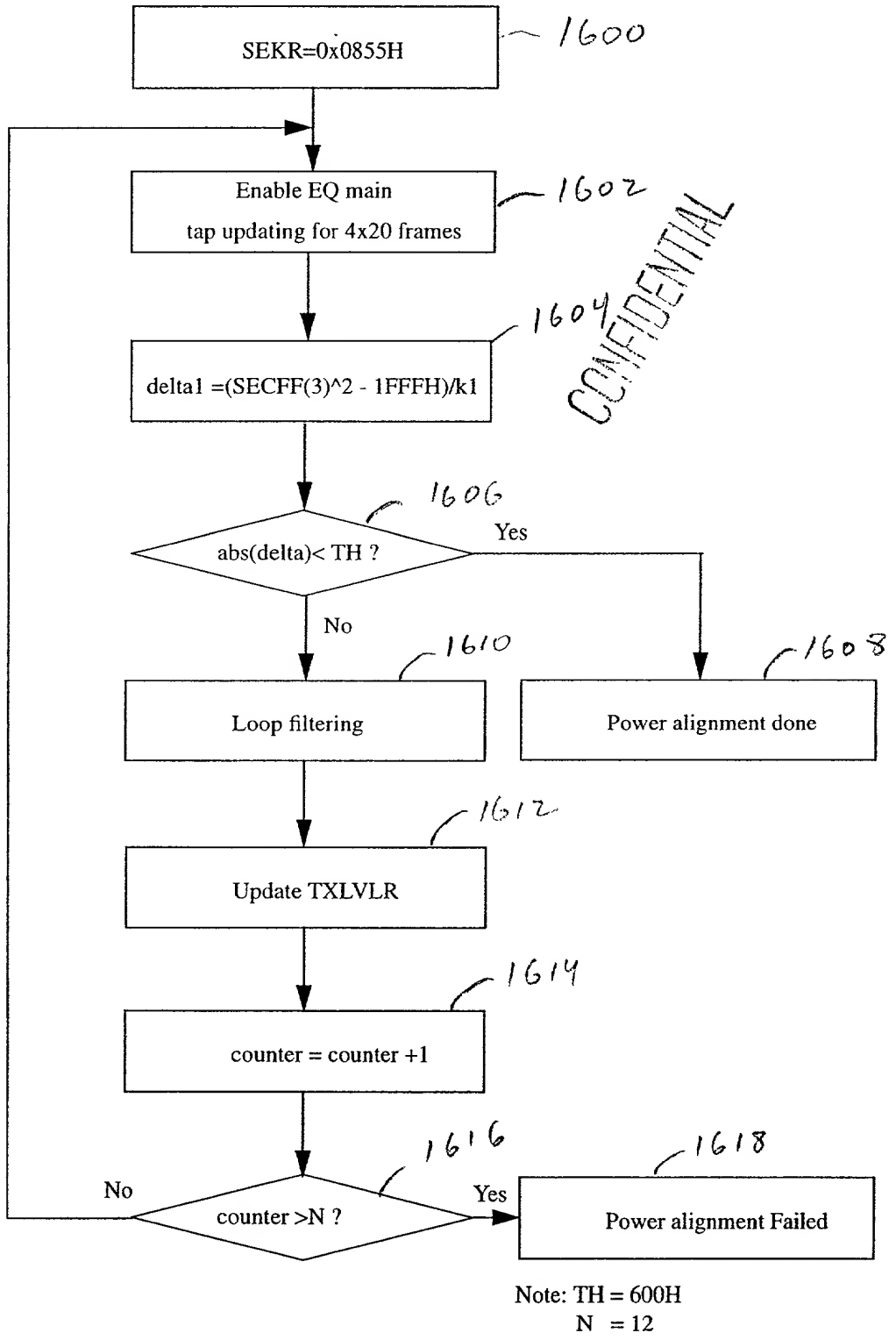


FIG. 6S

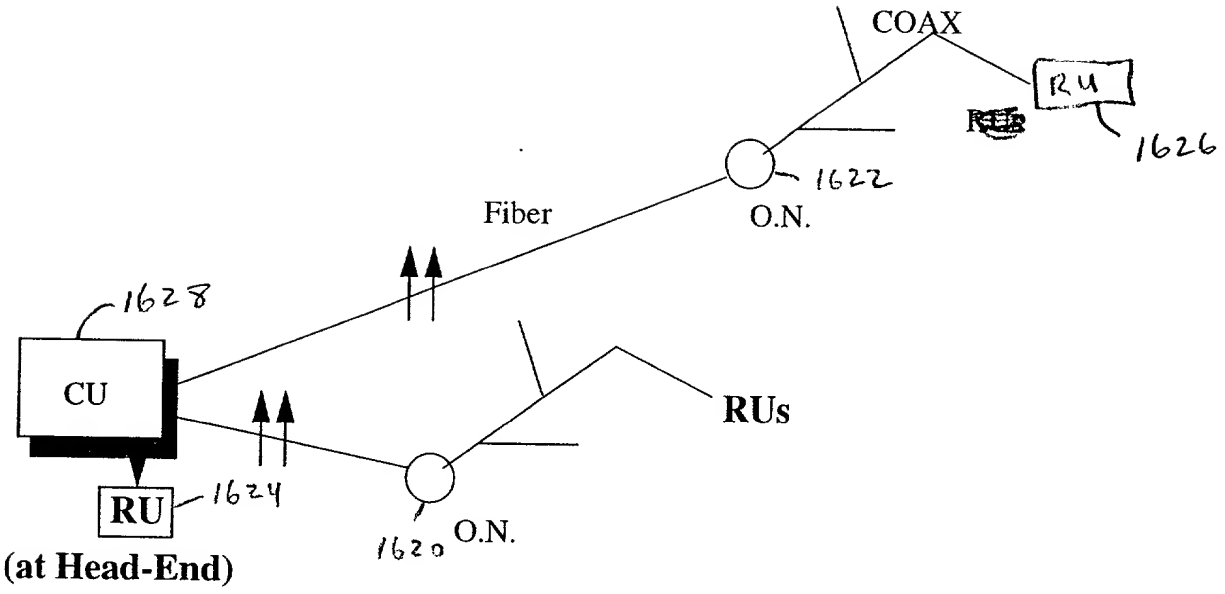
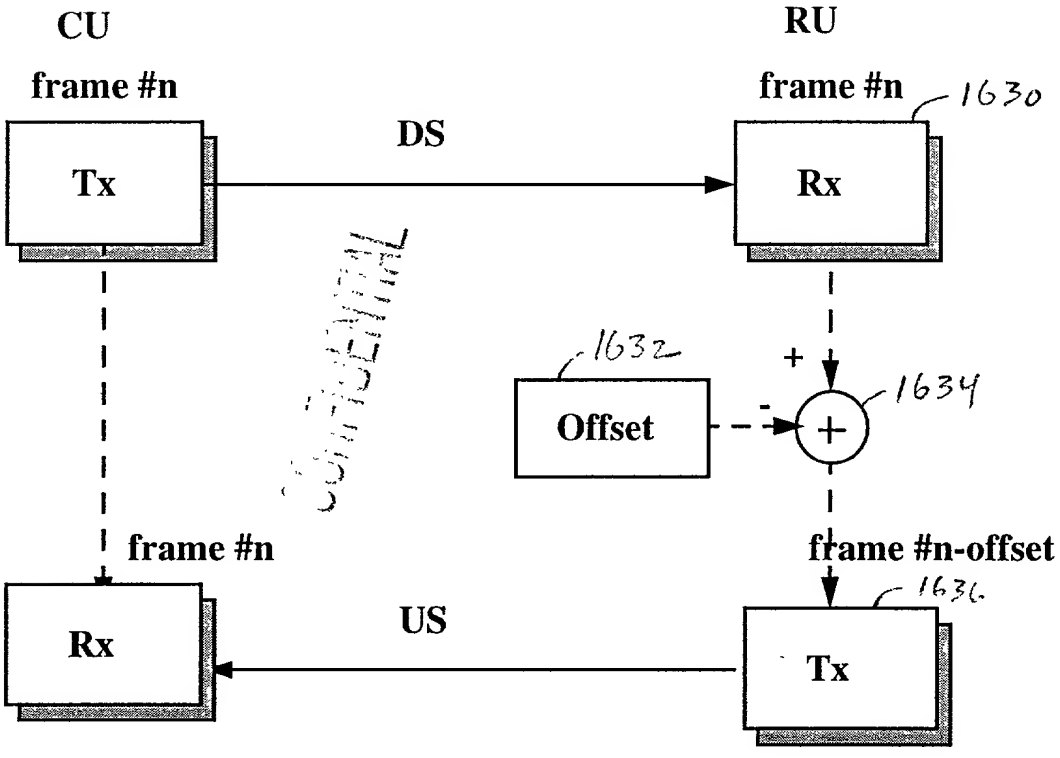


FIG. 66



Total Turn Around (TTA) in frames = Offset

FIG. 67

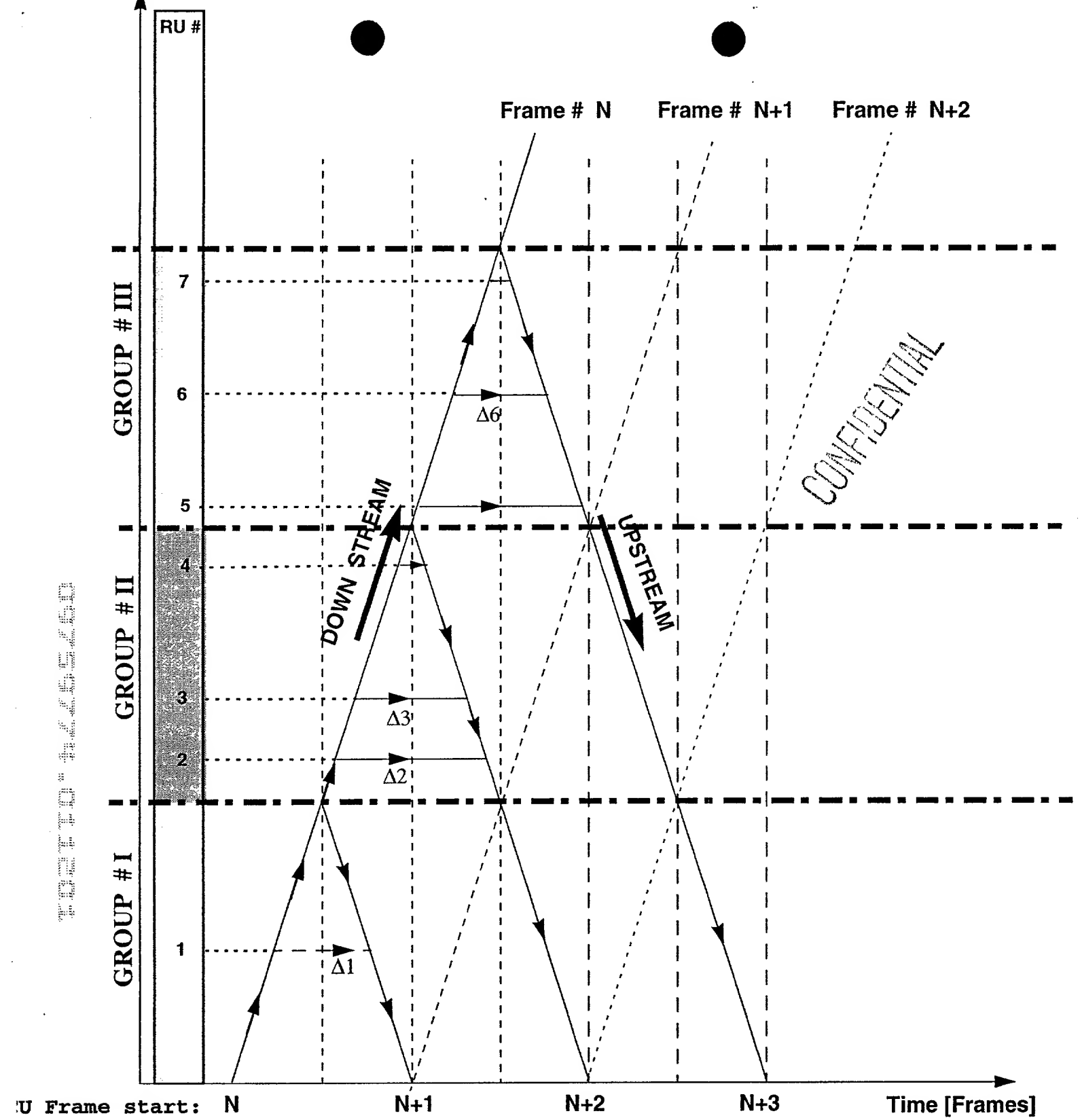


FIG. 68

Figure 3-1: Frame start propagation along the channel

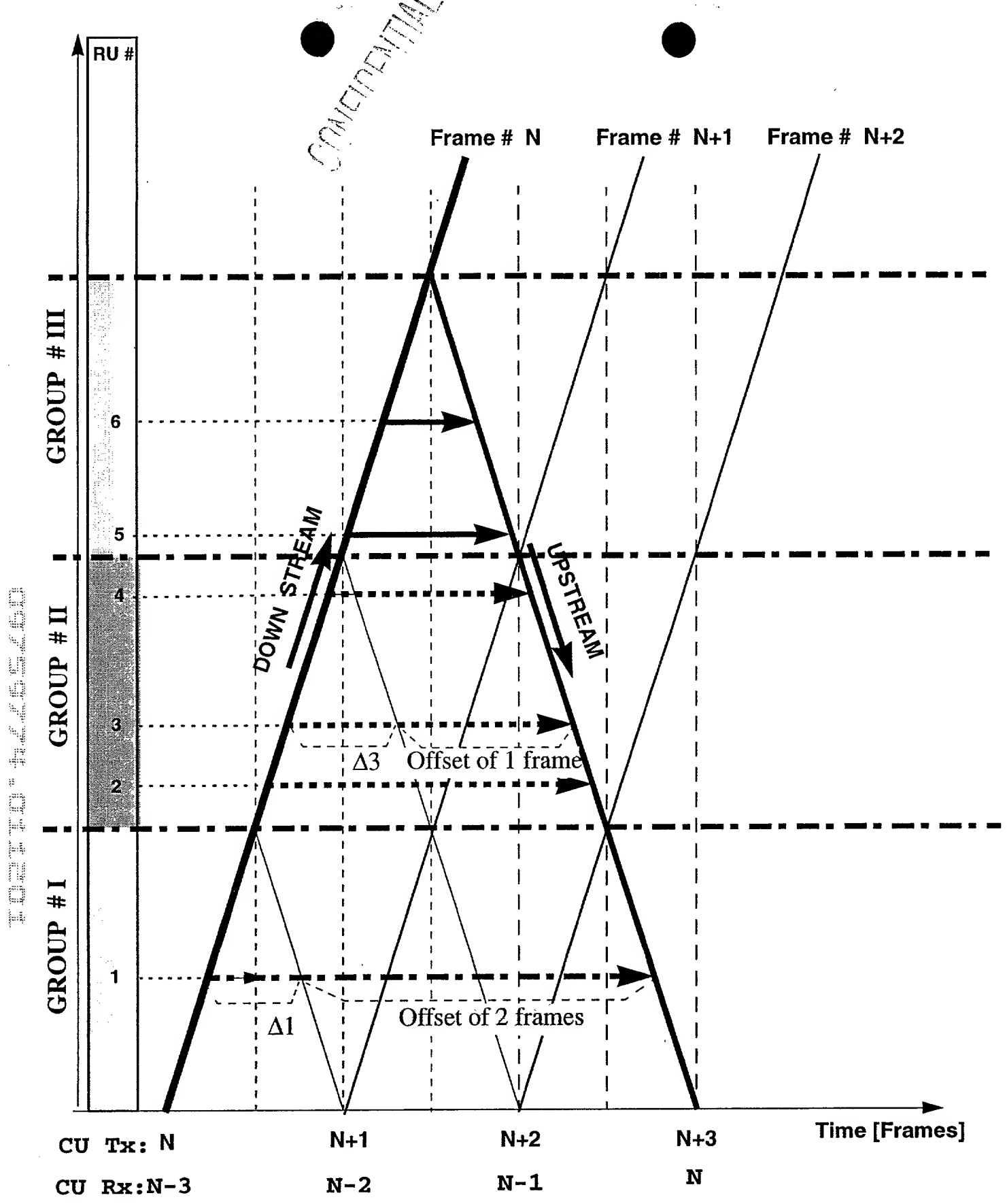


FIG. 69

Figure 69 Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

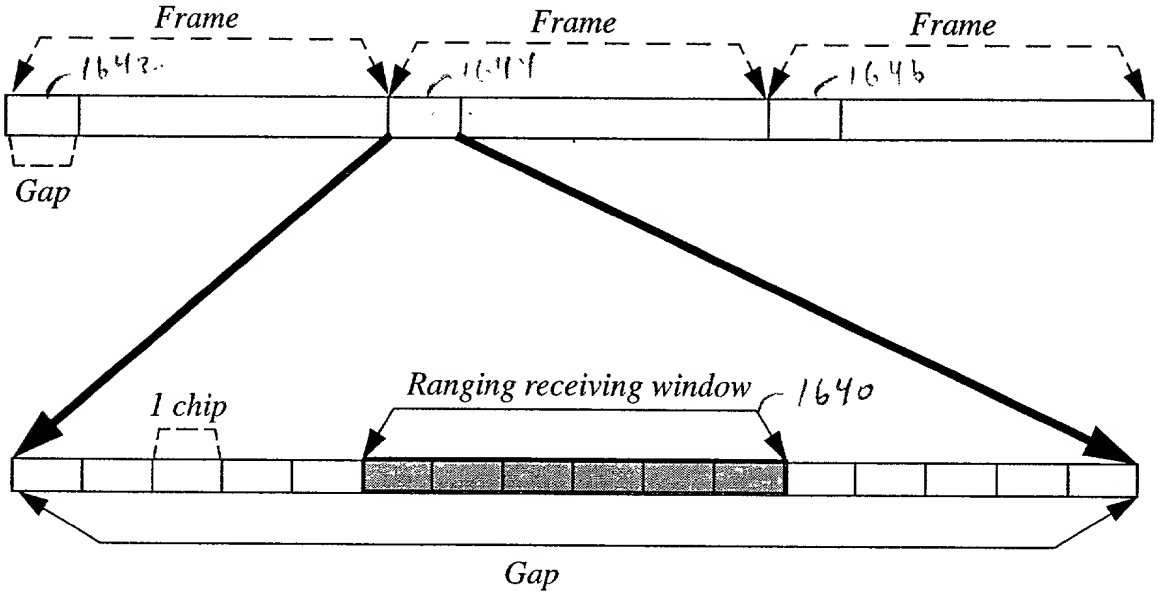

Frame
Frame
Frame
1642
1644
1646
Gap
1 chip
Ranging receiving window
1640
Gap

FIG. 70

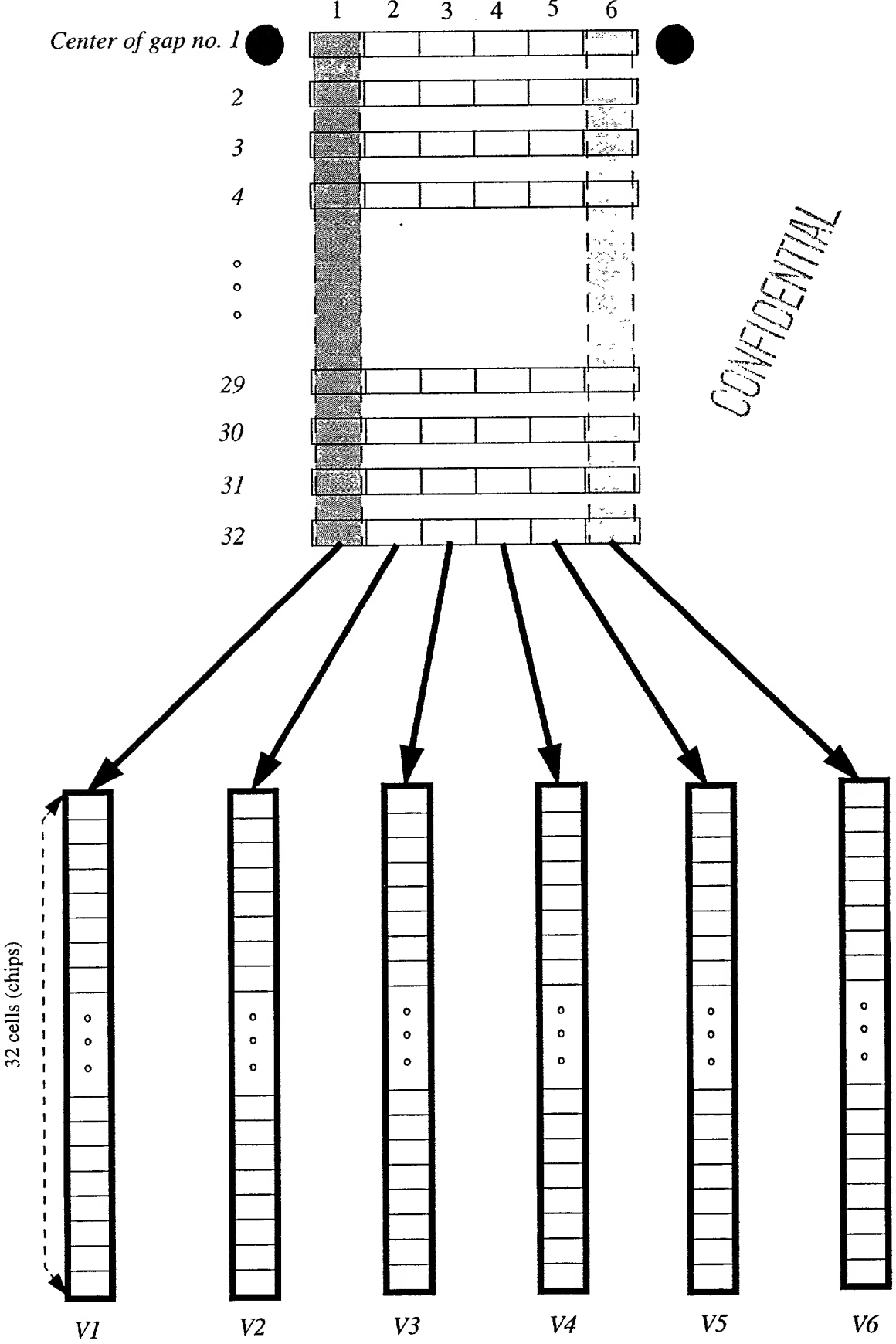


Figure 3.4: Overall view of the CU sensing windows in a "boundless ranging" algorithm

FIG. 71

Chip\FR	**1**	**2**	**3**	**4**	**5**	**6**	**7**		**33**
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**...**	**0**
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72